Maxim ADC App Notes

AN1041: Understanding Integrating ADCs

AN810: Understanding Flash ADCs

AN2102: Migrating from Integrating ADC Architectures to Sigma Delta

Understanding Integrating ADCs

Integrating analog-to-digital converters (ADCs) provide high resolution analog-to-digital conversions, with good noise rejection. These ADCs are ideal for digitizing low bandwidth signals, and are used in applications such as digital multi-meters and panel meters. They often include LCD or LED drivers and can be used stand alone without a microcontroller host. The following article explains how integrating ADCs work. Discussions include single-, dual- and multi-slope conversions. Also, an in-depth analysis of the integrating architecture will be discussed. Finally a comparisons against other ADC architectures will aid in the understanding and selection of integrating ADCs.

Integrating analog-to-digital converters (ADCs) provide high resolution and can provide good line frequency and noise rejection. Having started with the ubiquitous 7106, these converters have been around for quite some time. The integrating architecture provides a novel yet straightforward approach to converting a low bandwidth analog signal into its digital representation. These type of converters often include built-in drivers for LCD or LED displays and are found in many portable instrument applications, including digital panel meters and digital multi-meters.

Single-Slope ADC Architecture

The simplest form of an integrating ADC uses a single-slope architecture (Figures 1a and 1b). Here, an unknown input voltage is integrated and the value compared against a known reference value. The time it takes for the integrator to trip the comparator is proportional to the unknown voltage (T_{INT}/V_{IN}). In this case, the known reference voltage must be stable and accurate to guarantee the accuracy of the measurement.

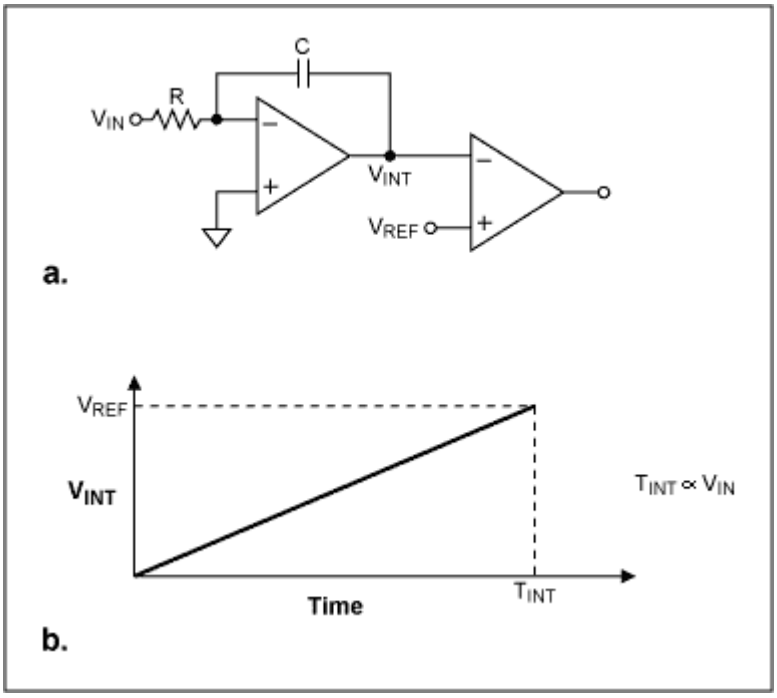

Figure 1a and 1b. Single-slope architecture

One drawback to this approach is that the accuracy is also dependent on the tolerances of the integrator's R and C values. Thus in a production environment, slight differences in each component's value change the conversion result and make measurement repeatability quite difficult to attain. To overcome this sensitivity to the component values, the dual-slope integrating architecture is used.

Dual-Slope ADC Architecture

A dual-slope ADC (DS-ADC) integrates an unknown input voltage (V_{IN}) for a fixed amount of time (T_{INT}), then "de-integrates" (T_{DEINT}) using a known reference voltage (V_{REF}) for a variable amount of time (see Figure 2).

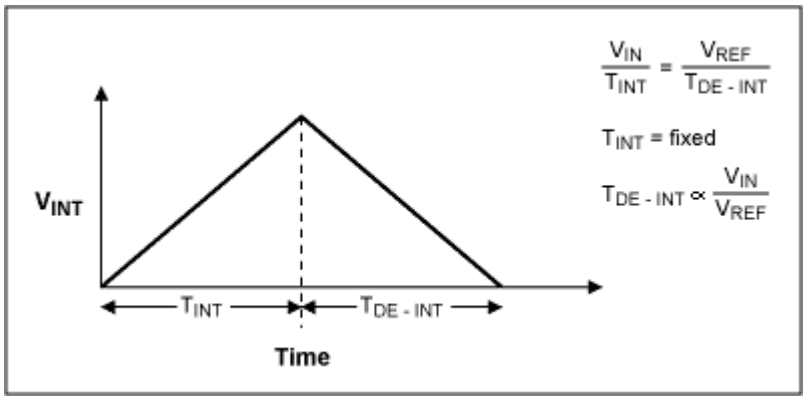

Figure 2. Dual-slope integration

The key advantage of this architecture over the single-slope is that the final conversion result is insensitive to errors in the component values. That is, any error introduced by a component value during the integrate cycle will be cancelled out during the de-integrate phase. In equation form:

$Vin / T_{INT} = V_{REF} / T_{DEINT}$

or

$T_{DEINT} = T_{INT} \cdot (V_{IN} / V_{REF})$

From this equation, we see that the de-integrate time is proportional to the ratio of V_{IN} / V_{REF}. A complete block diagram of a dual-slope converter is shown in Figure 3.

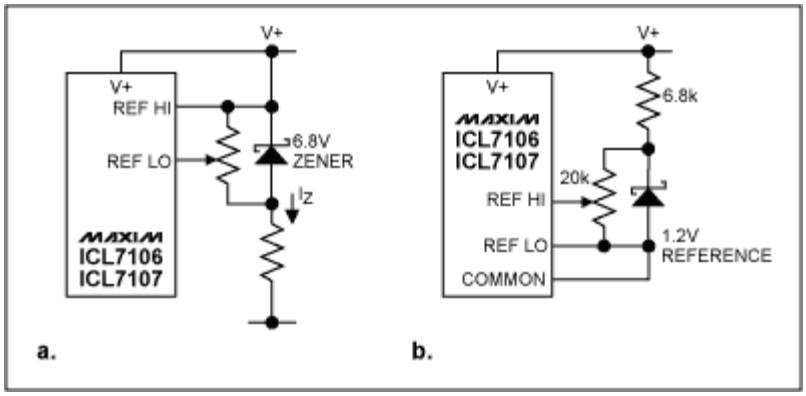

Figure 3. Dual-slope converter

As an example, to obtain 10-bit resolution, you would integrate for 1024 (2^{10}) clock cycles, then deintegrate for up to 1024 clock cycles (giving a maximum conversion of $2 \cdot 2^{10}$ cycles). For more resolution, increase the number of clock cycles. This tradeoff between conversion time and resolution is inherent in this implementation. It is possible to speed up the conversion time for a given resolution with moderate circuit changes. Unfortunately, all improvements shift some of the accuracy to matching, external components, charge injection, etc. In other words, all speed-up techniques have larger error budgets. Even in the simple converter in Figure 1, there are many potential error sources to consider (power-supply rejection [PSR], common-mode rejection [CMR], finite gain, over-voltage concerns, integrator saturation, comparator speed, comparator oscillation, "rollover", dielectric absorption, capacitor leakage current, parasitic capacitance, charge injection, etc).

Multi-Slope Integrating ADCs

The normal limit for resolution of the dual-slope architecture is based on the speed of the error comparator (this assumes the DC errors of the system have been minimized by designing for

high DC gain, and high PSR and CMR of the buffer, integrator and comparator). For a 20-bit converter (approximately 1 part in a million) and a 1MHz clock, the conversion time would be about 2 seconds. The ramp rate seen by the error comparator is about $2V/10^6$ divided by 1 microsecond. This is about 2 microvolts/microsecond. With such a small slew rate, the error comparator would allow the integrator to go well beyond its trip point by a considerable amount. This overshoot (measured at the integrator output) is called the "residue". This brute force technique is not likely to achieve a 20-bit converter.

Instead, we could convert the first 10 most significant bits (one integrate/de-integrate cycle), then amplify the residue by 2^5, then deintegrate again, then amplify the residue by 2^5, and then deintegrate for the last time. If the residue is correctly amplified (i.e., charge injection and other errors are small), this technique can be quite powerful in increasing the resolution and reducing the conversion time. Note the actual reading is: (Sum of the first deintegrate time $\cdot 2^{10}$) minus (sum of the second deintegrate time $\cdot 2^5$) plus (sum of the third deintegrate time $\cdot 2^0$).

In-Depth Architecture Analysis

Auto-Zero

In our previous analysis, we assumed an ideal converter. In actual practice, the circuit will have an offset that drifts over time and temperature. To minimize this affect, dual-slope converters employ an auto-zero phase. During autozeroing, the offset voltage of the buffer op amp the integrator and the comparator is measured and stored on an external capacitor. Thus, the integrate cycle effectively begins with a zeroed offset.

Line Rejection

One of the most attractive attributes of the DS-ADC is its rejection of unwanted 50/60Hz signals. If the integrate cycle lasts exactly time T , all frequencies of $N \cdot 1/T$ are completely rejected (theoretically). So for T = 100ms, multiples of 10Hz are rejected. The actual limitation of this rejection is due to the finite swing of the integrator (since we don't want it to saturate) and the inevitable "wobble" of the 50/60Hz frequency itself. Over a long period of time, 50/60Hz can be averaged to get extremely accurate time bases. Over a short time however, it jitters by a few Hertz. This will limit the actual line rejection to about 40-60dB.

Error Budget Analysis

DS-ADC's have a several terms in the error budget. This is primarily due to the high accuracy for which they are targeted.

The amplifiers must have high common-mode rejection (CMR), power supply rejection (PSR) and high finite gain (so the buffer can adequately drive its resistive load and the integrator its capacitive load). The full-scale integrate current [V_{IN}(max) / R_{INT}] is typically 20-100 microamps. This value is a tradeoff between low power and overcoming the effects of PC board leakage current. Some engineers have tried class B amplifiers for these op amps to save supply current. However, the inevitable crossover distortion must be carefully analyzed, as it can easily be larger than all other errors.

The comparator needs to respond within a fraction of a clock cycle to the fairly small signal. The signal is dependent on the slew rate during deintegrate ($I / C = V_{REF} / (R_{INT} * C_{INT})$). As the resolution goes up, this signal can be sub millivolt/microsecond. Unintentional hysteresis must be minimized as this causes "rollover". Rollover is defined as the difference between a near positive full-scale reading and near negative full-scale reading. The parameter is usually specified in the DS data sheet electrical specifications and is tested by simply applying a full-scale positive voltage, then applying a full-scale negative voltage, and then adding the results.

One of the most useful techniques for error reduction is accomplished by shorting the input terminals and taking a measurement. If the ADC design uses up/down counters as accumulators, then the measurement error can be easily subtracted from the input signal (V_{IN}) conversion result. This technique is not always acceptable as it doubles the conversion time if calibration is done prior to every conversion. However, it can correct for many more errors than just the offset error (such as delay of the internal comparator(s), charge injection, etc.).

External Components

A user has to supply the IC with a resistor (for converting the input voltage to a current), an integrator capacitor and an autozero capacitor. Both capacitors needed exceptional DA (dielectric absorption). A model of the integrator capacitor shown in Figure 4 shows the capacitor made up of high value, series R'C' components (caused by the relaxation of the dielectric) in parallel with the main capacitor. These series RC elements cause the capacitor to behave as if it had "memory". For example, suppose a capacitor was charged up to 1.000 Volts for an indefinite time, then shorted out for 10 time constants (SW1 moved to position 1). When the switch is moved to position 3, the capacitor "relaxes" to a voltage other than zero volts due to the "memory" effect. This phenomenon ultimately limits the accuracy, resolution and step response of the converter.

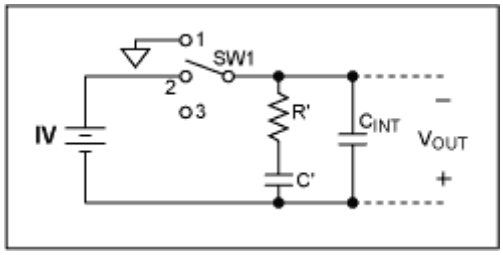

Figure 4. Model of the integrating capacitor

Versus Other ADC Architectures

We now will look at the integrating ADC versus a SAR and sigma-delta ADC. The flash and pipeline ADC architectures will be ignored since they rarely (if ever) compete against the slower speed integrating architecture.

Versus Successive Approximate Register (SAR) ADC

Both the SAR and integrating architectures work well with low bandwidth signals. The SAR ADC has a much wider bandwidth range, as they easily can convert signals at speeds in the low MHz range, while the integrating architecture is limited to about 100 samples/sec. Both architectures have low power consumption. Since SAR ADCs can be shut down between conversions, the effective power consumption is similar to the integrating ADC (to the first order). The biggest difference between the two converters is the common mode rejection and the number of external components required. Because the user sets the integration time, unwanted frequencies, such as 50Hz or 60Hz can effectively be notched out. The SAR ADC does not allow this. In addition, since integration basically is a method of averaging, the integrating ADC typically will have better noise performance. A SAR ADC has code-edge noise and spurious noise that is converted will have a more adverse affect with the SAR ADC than with the integrating ADC.

The integrating ADC easily converts low-level signals. Since the integrator ramp is set by the value of the integrating resistor, it is fairly easy to match the input signal range to the ADC. Most SARs expect a large signal at the ADC input. Thus for small (i.e., mV) signals, front-end signal conditioning circuitry is required.

The integrating ADC needs more external components than the SAR. A SAR typically needs a couple bypass capacitors. The integrating ADC requires a good integrating and reference capacitors and also a low-drift integrating resistor. In addition, the reference voltage is often a non-standard value (like 100mV or 409.6mV) so a reference voltage divider circuit is often used.

Versus Sigma-Delta ADC

The sigma-delta ADC uses oversampling to obtain very high resolution. It also allows input bandwidths in the low MHz range. Like the integrating ADC, this architecture can have excellent line rejection. It also provides a very low-power solution and it allows low level signals to be converted. Unlike the integrating ADC, the sigma-delta does not require any external components. In addition, it requires no trimming or calibration due to its digital architecture. Due to the oversampling nature and the fact that the sigma delta includes a digital filter, an anti-aliasing filter often is not required on the front end. Sigma-delta converters typically are available in 16-bit to 24-bit bit resolutions while integrating ADCs target the 12-bit to 16-bit range. Due to its straightforward architecture and its maturity, integrating ADCs are fairly inexpensive especially at the 12-bit level. However, at 16-bits, the sigma-delta also provides a low cost solution.

Application Note 810: Oct 02, 2001

Understanding Flash ADCs

Flash analog-to-digital converters, also known as parallel ADCs, are the fastest way to convert an analog signal to a digital signal. Flash ADCs are ideal for applications requiring very large bandwidth, however, they typically consume more power than other ADC architectures and are generally limited to 8-bits resolution. Flash ADCs are made by cascading high-speed comparators. Each comparator represents 1 LSB, and the output code can be determined in one compare cycle. This tutorial will also talk about flash converters vs. other converter types.

Flash analog-to-digital converters, also known as parallel ADCS, are the fastest way to convert an analog signal to a digital signal. They are suitable for applications requiring very large bandwidths. However, flash converters consume a lot of power, have relatively low resolution, and can be quite expensive. This limits them to high frequency applications that typically cannot be addressed any other way. Examples include data acquisition, satellite communication, radar processing, sampling oscilloscopes, and high-density disk drives.

Architecture Detail

Figure 1 shows a typical flash ADC block diagram. For an "N" bit converter, the circuit employs 2^N-1 comparators. A resistive divider with 2^N resistors provides the reference voltage. The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Each comparator produces a "1" when its analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator output is "0". Thus, if the analog input is between v_{x4} and v_{x5}, comparators x_1 through x_4 produce "1"s and the remaining comparators produce "0"s. The point where the code changes from ones to zeros is the point where the input signal becomes smaller than the respective comparator reference voltage levels.

This is known as thermometer code encoding, so named because it is similar to a mercury thermometer, where the mercury column always rises to the appropriate temperature and no mercury is present above that temperature. The thermometer code is then decoded to the appropriate digital output code.

The comparators are typically a cascade of wideband low gain stages. They are low gain because at high frequencies it's difficult to obtain both wide bandwidth and high gain. They are designed for low voltage offset, such that the input offset of each comparator is smaller than a LSB of the ADC. Otherwise, the comparator's offset could falsely trip the comparator, resulting in a digital output code not representative of a thermometer code. A regenerative latch at each comparator output stores the result. The latch has positive feedback, so that the end state is forced to either a "1" or a "0".

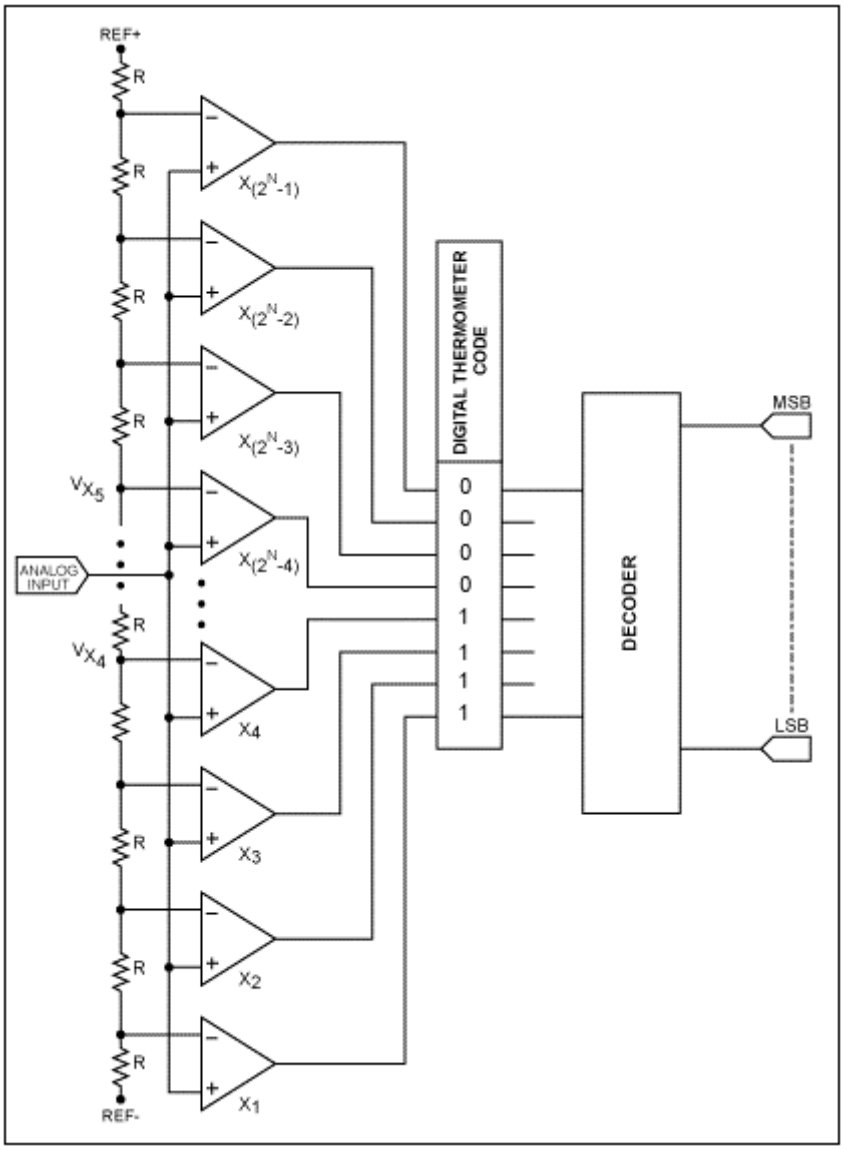

Figure 1. Flash ADC architecture

Some reality checks now need to be added to optimize the flash converter architecture.

Sparkle Codes

Normally, the comparator outputs will be a thermometer code, such as 00011111. Errors may cause an output like 00010111 (i.e., there is a spurious zero in the result). This out of sequence "0" is called a sparkle. This may be caused by imperfect input settling or comparator timing mismatch. The magnitude of the error can be quite large. Modern converters like the MAX104 employ an input track-and-hold in front of the ADC along with an encoding technique that suppresses sparkle codes.

Metastability

When a digital output of a comparator is ambiguous (neither a one nor a zero), the output is defined as metastable. Metastability can be reduced by allowing more time for regeneration. Gray-code encoding can also greatly improve metastability. Gray-code encoding allows only one bit in the output to change at a time. The comparator outputs are first converted to gray-code encoding and then later decoded to binary if desired.

Another problem occurs when a metastable output drives two distinct circuits. It is possible for one circuit to declare the input a "1" while the other circuit thinks it's a "0". This can create major errors. To avoid this, only one circuit should sense a potentially mestatable output.

Input Signal Frequency Dependence

When the input signal changes before all the comparators have completed their decision, the ADC performance is adversely impacted. The most serious impact is a drop-off in signal-to-noise ratio plus distortion (SINAD) as the frequency of the analog input frequency increases.

Measuring spurious free dynamic range (SFDR) is another good way to observe converter performance. The "effective bits" achieved is a function of input frequency. This can be improved by adding a track-and-hold (T/H) circuit in front of the ADC. This allows dramatic improvement, especially when input frequencies approach the Nyquist frequency, as shown in Figure 2 (taken from the MAX104 data sheet). Parts without the track-and-hold show a significant drop-off in SFDR.

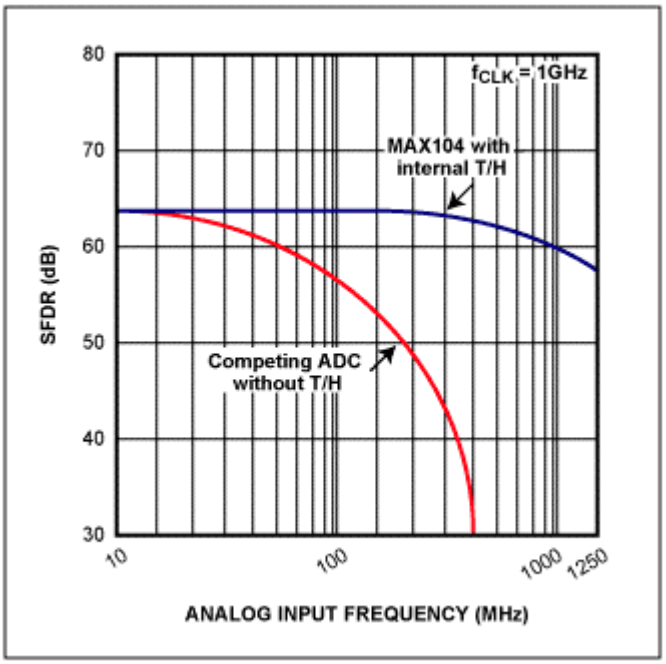

Figure 2. Spurious free dynamic range as a function of input frequency

Clock Jitter

Signal-to-noise ratio (SNR) is degraded when there is jitter in the sampling clock. This becomes noticeable for high analog input frequencies. To achieve accurate results, it is critical to provide the ADC with a low-jitter, sampling clock source.

Architecture Tradeoffs

ADCs can be implemented by employing a variety of architectures. The principal tradeoffs between these alternatives are:

- *The time it takes to complete a conversion (conversion time).* For flash converters, the conversion time does not change materially with increased resolution. The conversion time for Successive Approximation Register (SAR) or Pipelined converters increases approximately linearly with an increase in resolution (Figure 3a). For integrating ADCs, the conversion time doubles with every bit increase in resolution.
- *Component matching requirements in the circuit.* Flash ADC component matching typically limits resolution to around 8-bits. Calibration and trimming are sometimes used to improve the matching available on chip. Component matching requirements double with every bit increase in resolution.

This applies to flash, successive approximation or pipelined converters, but not integrating converters. For integrating converters, component matching does not materially increase with an increase in resolution (Figure 3b).

- *Die size, cost and power.* For flash converters, every bit increase in resolution almost doubles the size of the ADC core circuitry. The power also doubles. In contrast, a SAR, Pipelined, or sigma-delta ADC die size will increase linearly with an increase in resolution, and an integrating converter core die size will not materially change with an increase in resolution (Figure 3c). An increase in die size increases cost.

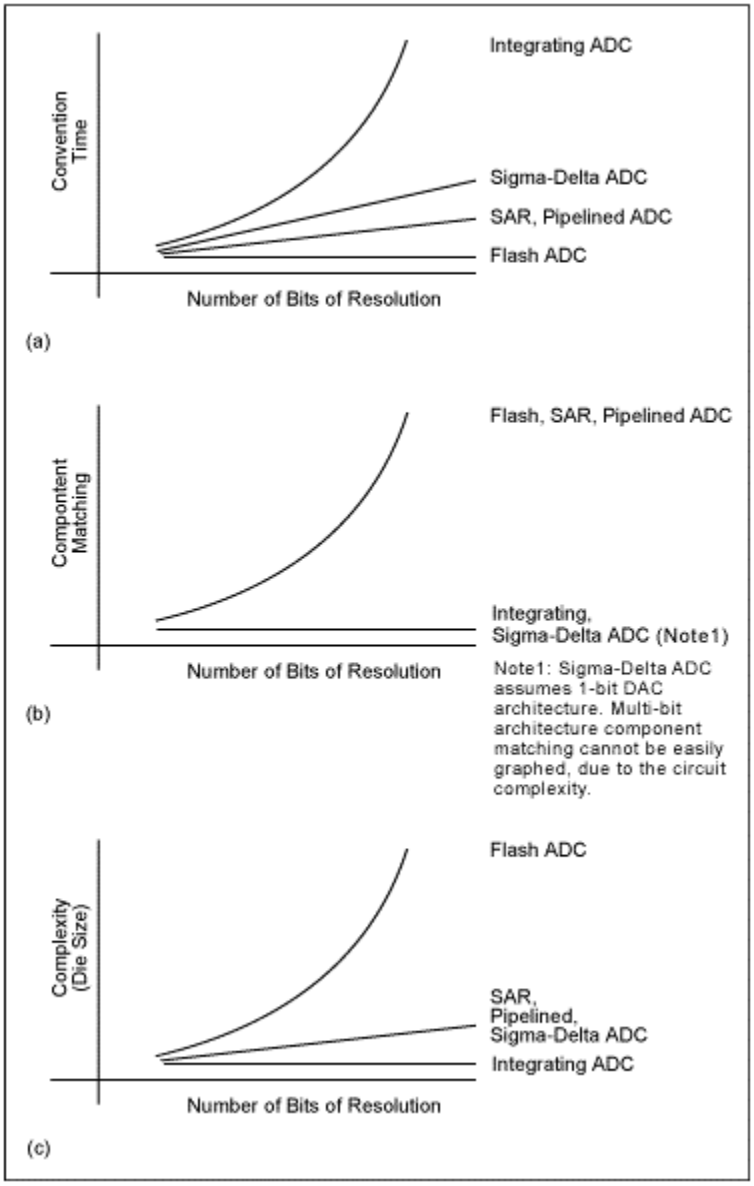

Figure 3. Architecture tradeoffs

FLASH ADC vs. Other ADC Architectures

Flash vs. Successive Approximation Register (SAR) ADCs

In a SAR converter, the bits are decided by a single high-speed, high-accuracy comparator one bit at a time (from the MSB down to the LSB), by comparing the analog input with a DAC whose output is updated by previously decided bits and thus successively approximates the analog input. This serial nature of the SAR

limits its speed to no more than a few Msps, while flash ADCs exceed giga-sample per second (Gsps) conversion rates.

SAR converters are available in resolutions up to 16-bits. An example of such a device is the MAX1132. Flash ADCs are typically limited to around 8-bits. The slower speed also allows the SAR ADC to be much lower in power. For example, the MAX1106, an 8-bit SAR converter, uses 100µA at 3.3V with a conversion rate of 25ksps. The MAX104 dissipates 5.25W. This is about 16,000 times higher power consumption compared to the MAX1106, but also 40,000 times faster in terms of its maximum sampling rate.

The SAR architecture is also less expensive. The MAX1106 at 1k volumes sells at approximately $1.51, while the MAX104 sells at roughly $398. Package sizes are larger for flash converters. In addition to a larger die size requiring a larger package, the package needs to dissipate a lot of power and needs many pins for power and ground signal integrity. The package size of the MAX104 is more than 50 times larger than the MAX1106.

Flash vs. Pipelined ADCs

A pipelined ADC employs a parallel structure in which each stage works on one to a few bits of successive samples concurrently. This improves speed at the expense of power and latency. However, each pipelined stage is much slower than a flash section. The pipelined ADC requires accurate amplification in the DACs and interstage amplifiers, and these stages have to settle to the desired linearity level. By contrast, in a flash ADC, the comparator only needs to be low offset and be able to resolve its inputs to a digital level (i.e., there is no linear settling time involved). However, some flash converters require preamplifers to drive the comparators. Gain linearity needs to be carefully specified.

Pipelined converters are capable of conversion speeds of around 100Msps at 8 to 14-bit resolutions. An example of a pipelined converter is the MAX1449, a 105MHz, 10-bit ADC. For a given resolution, pipelined ADCs are around 10 times slower compared to flash converters of similar resolution. Pipelined converters are possibly the optimal architecture for ADCs that need to sample at rates up to around 100Msps with resolution at 10-bits and above. At resolutions of up to 10-bits, and conversion rates above a few hundred Msps, flash ADCs dominate.

Interestingly, there are some situations where flash ADCs are hidden inside a converter employing another architecture to increase its speed. This is the case, for example, in the MAX1200; a 16-bit pipelined ADC that includes an internal 5-bit flash ADC.

Flash vs. Integrating ADCs

Single, dual and multi-slope ADCs can achieve high resolutions of 16-bits or more are relatively inexpensive and dissipate materially less power. These devices support very low conversion rates, typically less than a few hundred samples per second. Most applications are for monitoring DC signals in the instrumentation and industrial markets. This architecture competes with sigma-delta converters.

Flash vs. Sigma-Delta ADCs

Flash ADCs do not compete with this architecture because currently the achievable conversion rates differ by up to two orders of magnitude. The sigma-delta architecture is suitable for applications with much lower bandwidth, typically less than 1MHz, with resolutions in the 12 to 16-bit range. These converters are capable of the highest resolution possible in ADCs. They require simpler anti-alias filters (if needed) to bandlimit the signal prior to conversion.

They trade speed for resolution by oversampling, followed by filtering to reduce noise. However, these devices are not always efficient for multi-channel applications. This architecture can be implemented by using sampled data filters (also known as modulators) or continuous time filters. For higher frequency conversion rates the continuous time architecture is potentially capable of reaching conversion rates in the hundreds of Msps range with low resolution of 6 to 8-bits. This approach is still in the early research and development stage and offers competition to flash alternatives in the lower conversion rate range.

Another interesting use of a flash ADC is as a building block inside a sigma-delta circuit to increase the conversion rate of the ADC.

Sub-Ranging ADCs

When higher resolution converters or smaller die size and power for a given resolution are needed, multi-stage conversion is employed. This architecture is known as a sub-ranging converter. This is also sometimes referred to as a multi-step or half-flash converter. This approach combines ideas from successive approximation and flash architectures.

Sub-ranging ADCs reduce the number of bits to be converted into smaller groups, which are then run through a lower resolution flash converter. This approach reduces the number of comparators and reduces the logic complexity, compared to a flash converter (Figure 4). The tradeoff results in slower conversion speed compared to flash.

The MAX153 is an 8-bit, 1Msps ADC implemented with a sub-ranging architecture. This circuit employs a two-step technique. Here a first conversion is completed with a 4-bit converter. A residue is created, where the result of the 4-bit conversion is converted back to an analog signal (with an 8-bit accurate DAC) and subtracted from the input signal. This residue is again converted by the 4-bit ADC and the results of the first and second pass are combined to provide the 8-bit digital output.

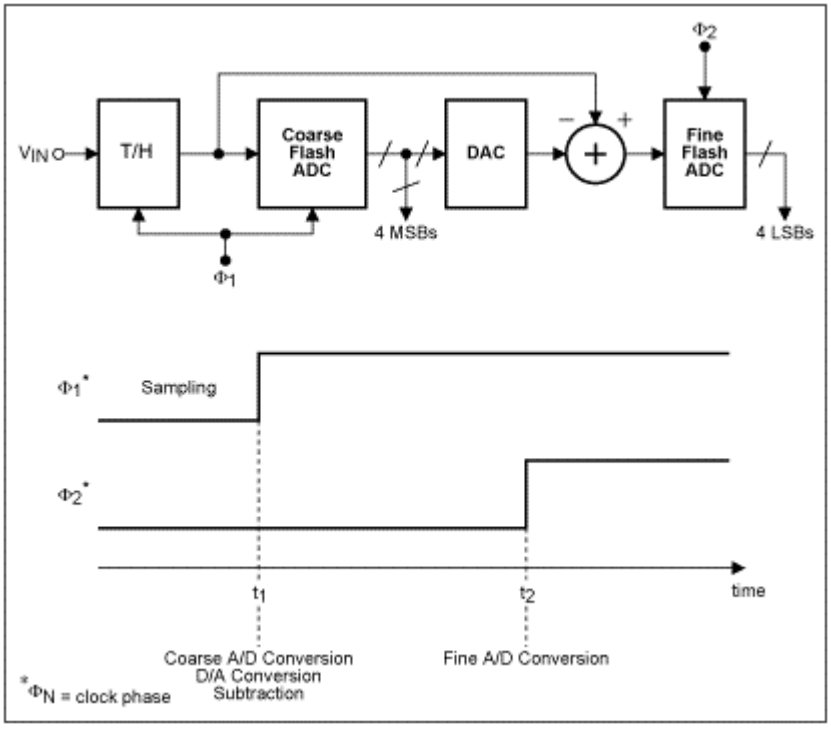

Figure 4. Sub-ranging ADC architecture

Process Technology

The fastest monolithic converters are built using bipolar technology. Flash converter speeds are currently in excess of 1Gsps. Examples are the MAX104/MAX106. CMOS flash converters are available at lower speed and resolutions compared to bipolar technology offerings and are typically intended for integration into a larger CMOS circuit. CMOS, BiCMOS and bipolar technologies will continue to improve, yielding increasingly higher conversion rates.

Conclusion

For applications requiring modest resolutions, typically up to 8-bits, at sampling frequencies in the high hundreds of MHz, the flash architecture may be the only viable alternative. The user must supply a low-jitter clock to ensure good ADC performance. For applications with high analog input frequencies, the ADC chosen should have an internal track-and-hold.

Application Note 2102: June 12, 2003

Migrating from Integrating ADC Architectures to Sigma Delta

This article compares the merits of integrating and sigma delta ADC architectures for panel meter applications. It focuses on the difficult-to-understand concepts of over-sampling, noise shaping, and decimation filtering. It includes a description of a new family of panel-meter-specific ICs, the MAX1491-MAX1499.

Integrating Architecture

An integrating converter architecture combines high resolution and excellent noise rejection, making it ideal for converting low-bandwidth analog signals. Integrating ADCs reject both high frequency noise and 50/60Hz noise.

If the integrate cycle time = T, then all frequencies of N 1/T are completely rejected (theoretically). T can be chosen to reject 50/60Hz noise. Since an analog integrator is effectively a low pass filter, all input signals with periods significantly shorter then T average out to zero. For digital panel meter applications, a wide selection of integrating ADCs with built-in LED and LCD drivers are available to provide a stand-alone solution. The ICL71xx industry-standard integrating ADCs are showing their age, but improved parts are available.

The performance of integrating ADCs relies on precision integration and de-integration cycles, which requires precision external components. The most critical components are auto-zeroing and integrating capacitors. Both of these capacitors require exceptional dielectric absorption characteristics to reduce the memory effect, which ultimately limits accuracy. These high performance capacitors are costly and are susceptible to leakage currents, so careful PCB layout and cleaning are required.

Some of these parts require dual supplies, which add additional cost. For smaller form factors, die packaging was often the only solution. An external zener diode, reference created the ADC's reference voltage. Non-linear input signals need specialized signal conditioning to convert the signal to ±2V or ±200mV, for displaying on the LED or LCD panel.

Sigma-Delta Converters

Sigma-delta converters are also well suited for low bandwidth, high-resolution acquisition. Panel meter designers often choose integrating ADCs because they are familiar and widely available. Sigma delta converters combine a simple analog modulator with a more complex digital filter.

Accuracy depends on the noise and linearity performance of the modulator, which uses high performance amplifiers. They are not dependent on highly accurate external components. Smaller process geometries have allowed IC manufacturers to integrate references, clock sources, charge pumps and display drivers while remaining economical.

The digital filter converts the analog modulator output to the digital output word and also provides lowpass filtering. In panel meter applications, a $Sinc^3$ filter response with notches at 50 and 60Hz excellent (>100dB) 50/60Hz rejection. However, one disadvantage inherent in the sigma-delta architecture is that the filter does not provide attenuation at integer multiples of the modulator sampling frequency. The modulator frequency is based on the over sampling ratio (OSR) x data output rate. In practice, large oversampling ratios result in the modulator sampling frequency being well above the bandwidth of the input signal. Anti-aliasing filter can be omitted without degrading system performance if the magnitude of the input signal at the modulator sampling frequencies is small.

The MAX1491-MAX1499 utilizes a Sigma Delta Architecture and is an excellent choice for panel meter applications. It features an integrated oscillator, an internal 2.048V bandgap reference (20ppm/°C typical) and an on-chip charge pump that internally generates a negative supply for the BI-polar, high impedance input buffers (>1GΩ typical). These 20-bit sigma delta based ADCs include low battery warning, peak detector and hold function. For ±2V input range, the oversampling ratio is 128 and for the ±200mV input range, the oversampling ratio is 1024.

Optional SPI™/QSPI™/MICROWIRE™ compatible serial interface increases flexibility. In additiona to replacing dip-switches and jumpers needed to configure the panel meter, a µC interface allows for linearization or table lookup of the conversion result using a cheap µC before displaying the output. Non-linear measurements such as thermocouple measurements, thermistor measurements or pH no longer require complex analog linearization. Use the table below select the suggested functional equivalent of the integrating panel meter ICs.