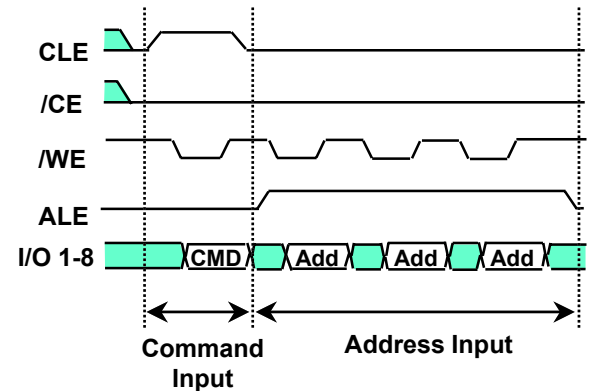
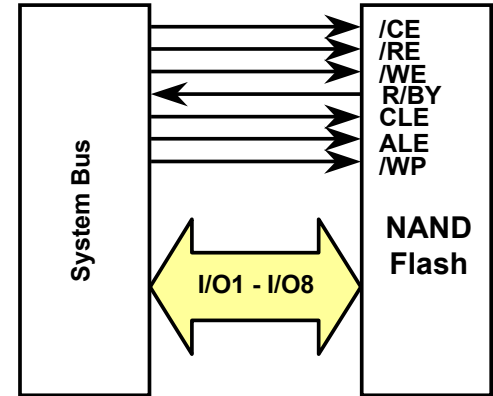


What is NAND Flash Memory?

March '03

File Memory Marketing & Promotion Department
Memory Division
TOSHIBA Semiconductor Company

- **Suitable for file storage**
 - File memory architecture
 - Page programming (512 bytes/page)
- **High performance**
 - High speed programming and erasing
- **Low cost**
 - Small chip size based on NAND Structure
 - Small pin count
- **Easy memory expansion**
 - Simple interface by command control

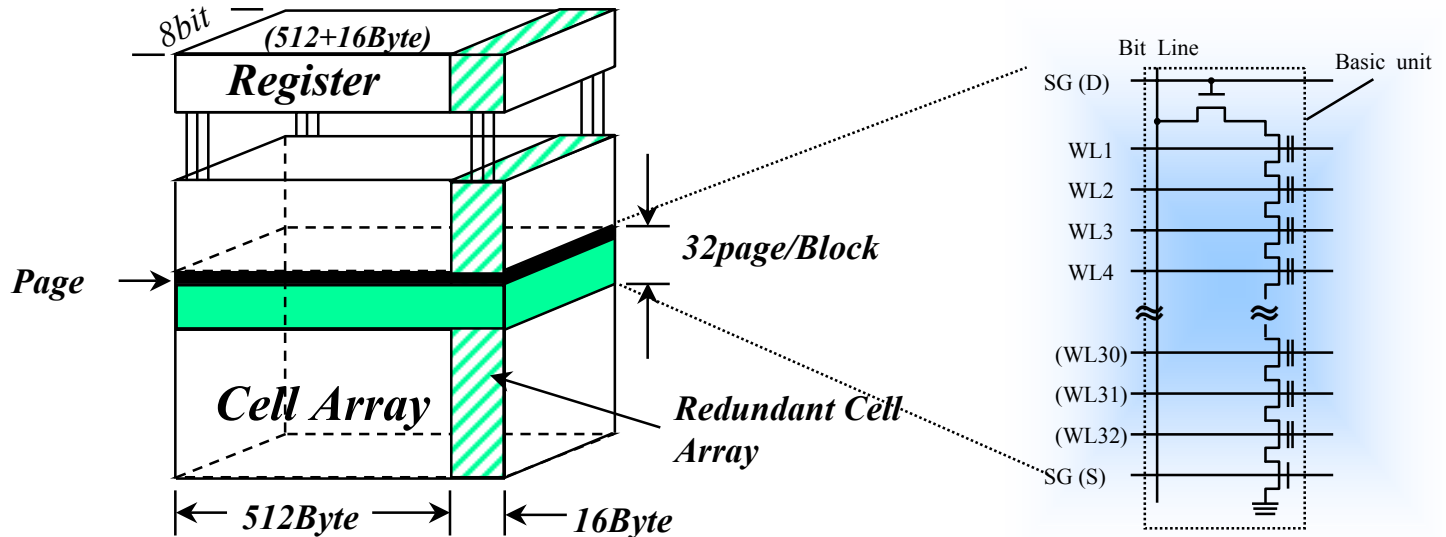


	NAND	NOR
Cell Array	<p>Word line</p> <p>Unit Cell</p> <p>Source line</p>	<p>Bit line</p> <p>Word line</p> <p>Contact</p> <p>Unit Cell</p> <p>Source line</p>
Layout	<p>$2E$</p> <p>$2F$</p>	<p>$2E$</p> <p>$5F$</p>
Cross-section		
Cell size	$4F^2$	$10F^2$

	NAND	NOR
Capacity	~ 1Gbit (2chips/pkg)	~ 128Mbit
Power Supply	2.7-3.6V	2.3-3.6V
I/O	x8	x8/x16
Access Time	50ns(serial access cycle) 25μs(random access)	70ns(30pF, 2.3V) 65ns(30pF, 2.7V)
Program Speed (typ.)	————	8μs/Byte
	200μs/512Byte	4.1ms/512Byte
Erase Speed(typ.)	2ms/Block (16KB)	700ms/Block
Prog+Erase(typ.)	33.6ms / 64KB	1.23s/Block (main:64KB)

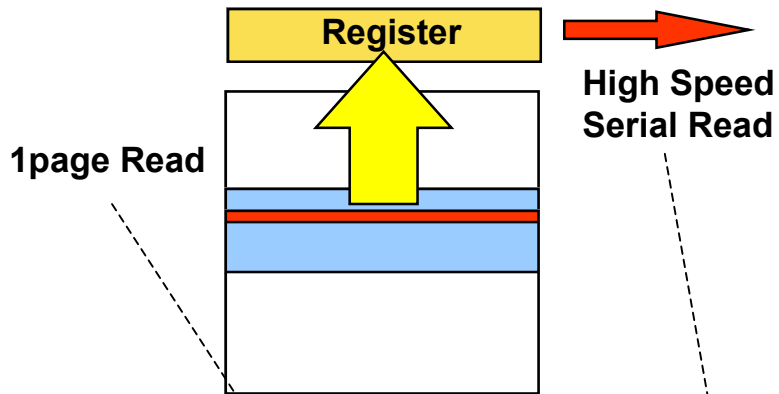
NAND Flash Memory Block Diagram

ex.256Mb NAND Flash Memory

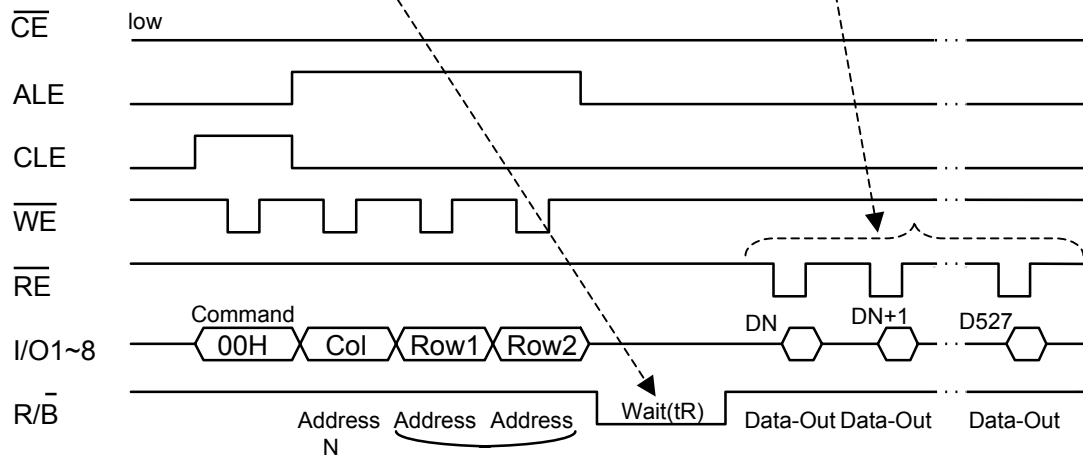


256Mb NAND Flash
Page Size : 512+16 Bytes
Block Size : 16KBytes
of Blocks : 2048 Blocks

Read

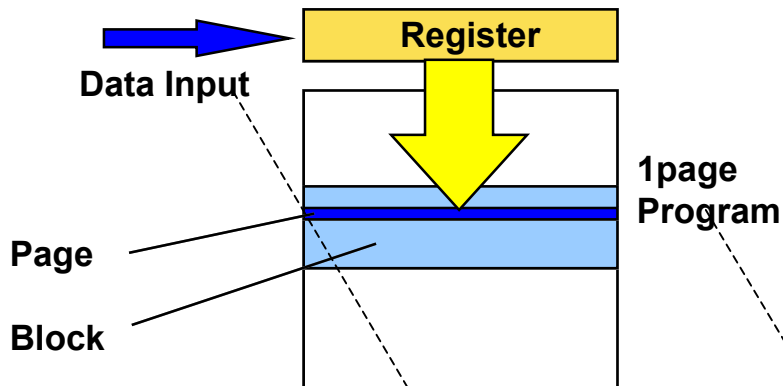


< Timing Chart >

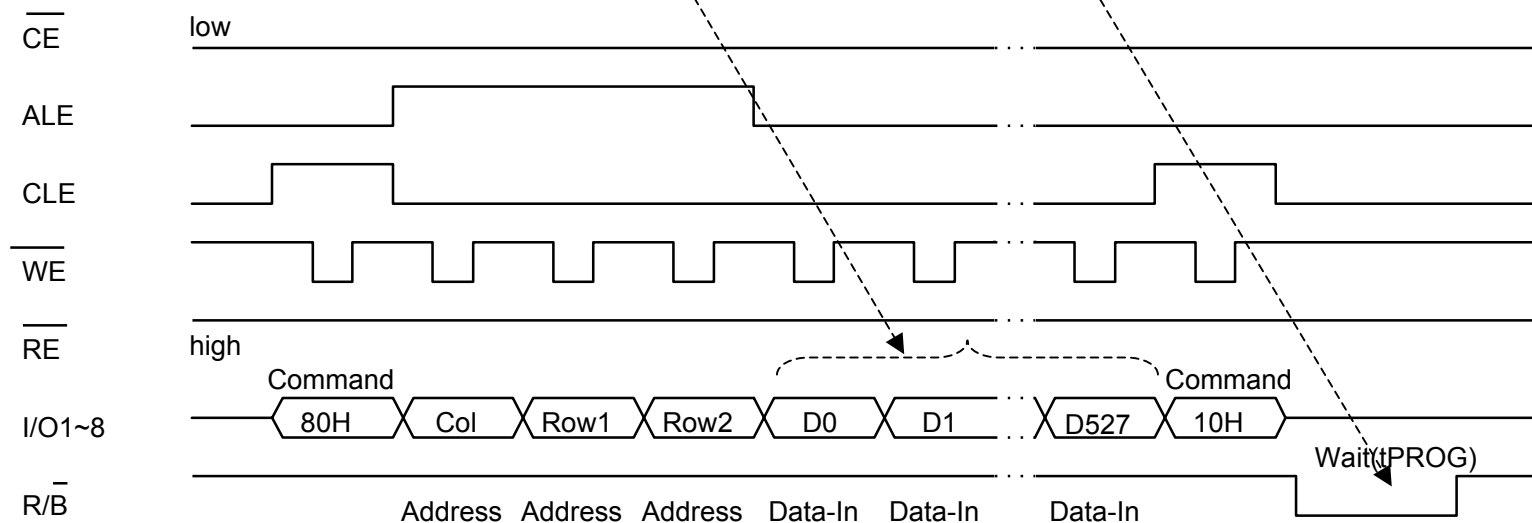


(ex. 256Mb NAND Flash Memory)

Program

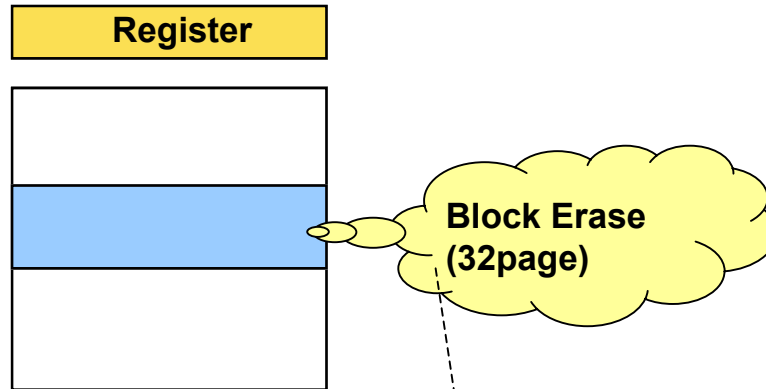


< Timing Chart >

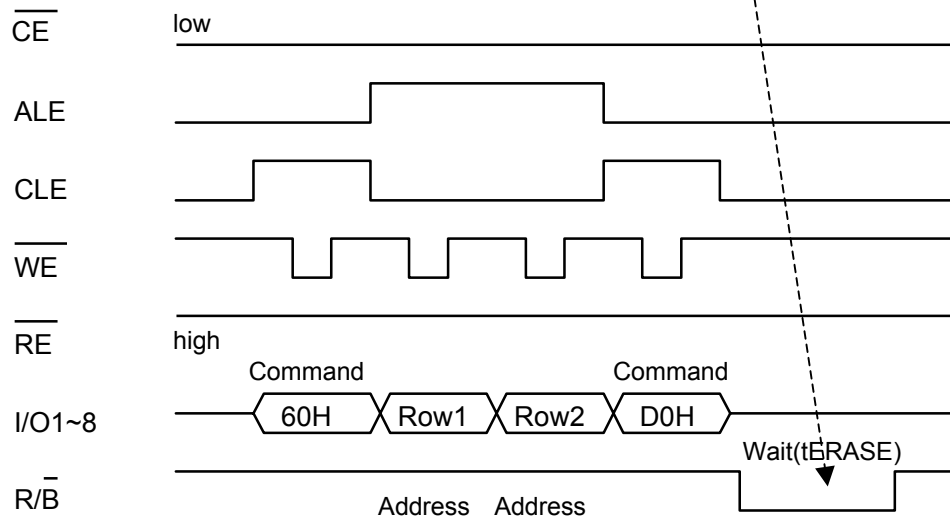


(ex. 256Mb NAND Flash Memory)

■ Erase



< Timing Chart >



(ex. 256Mb NAND Flash Memory)

< Required Items >

1. NAND Flash File Management

- Bad Block Management
- Wear Leveling Treatment

2. ECC Support

- 1 bit/page error correction
and 2bit/page error detection**

* ECC : Error Correction Code

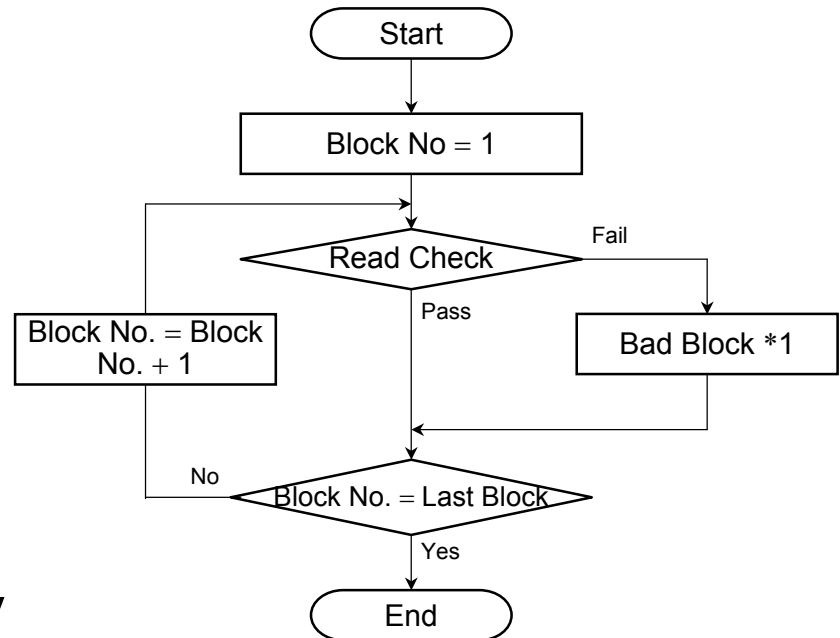
** : 2LC NAND Flash 1bit/page ECC

Number of valid blocks at shipping

Type.	Min.	Max.
TC58V64	1014	1024
TC58128	1004	1024
TC58256	2008	2048
TC58512	4016	4096
TH58100	8032	8192

Invalid blocks have to be detected by bad block test flow before erasing.

- Invalid block : include "0" data. This "0" data may be lost by erasing.
- Valid block : has only "1" data.



< Read Check >

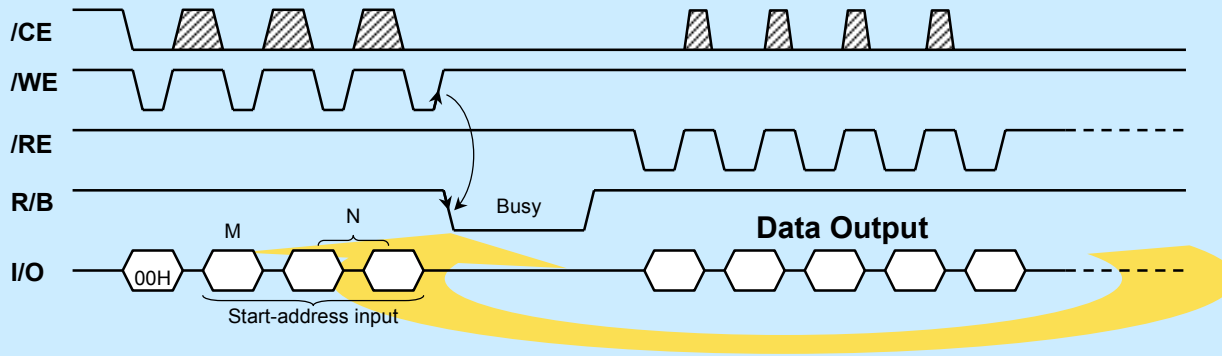
Read the 1st page of each block. If byte 517 of the 1st page is not FF (Hex), define the block as a bad block. The 1st block in the device is guaranteed to be good at time of shipment.

*1 : No erase operation is allowed to bad blocks

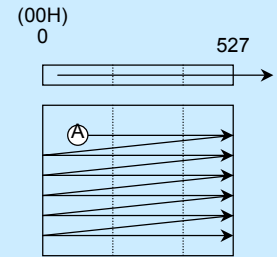
	0.16um				
	TC58V64BFT	TC58128AFT	TC58256AFT	TC58512FT	TH58100FT
	64Mb	128Mb	256Mb	512Mb	1Gb
Density	(8M+256K)x8	(16M+512K)x8	(32M+1M)x8	(64M+2M)x8	(128M+4M)x8
Operation voltage	2.7V-3.6V	←	←	←	←
Page size (program unit)	512B+16B	←	←	←	←
Block size (erase unit)	8KB+256B	16KB+512B	←	←	←
Number of Pages per Block	16	32	←	←	←
Number of Blocks	1024	1024	2048	4096	8192
Number of Address cycle	3	←	←	4	←
Random access time (us)	25us (max.)				
Serial access time (ns)	50ns (min.)				
Package	400mil / 0.8mm TSOP type II	TSOP I 48-P-1220-0.50			

2 Type Read Function

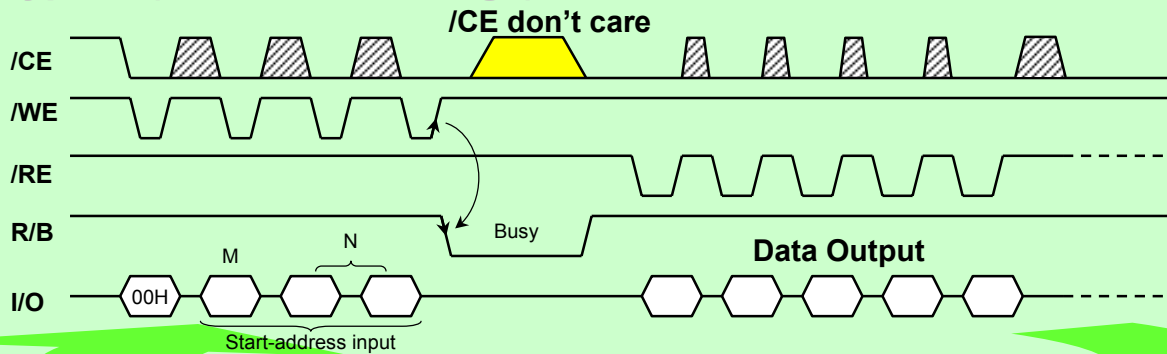
Type 1 (TSOP Package)



Sequential Read



Type 2 (BGA/MCP Package)



No Sequential Read

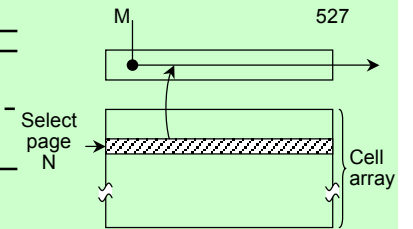


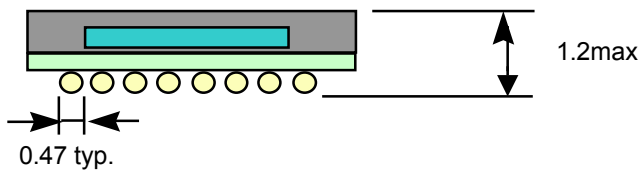
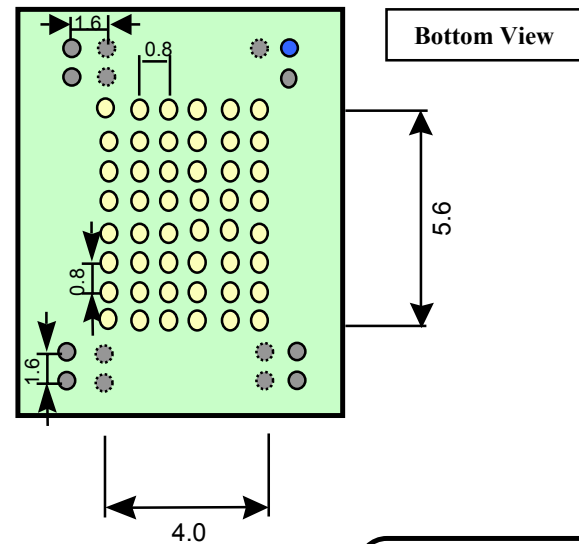
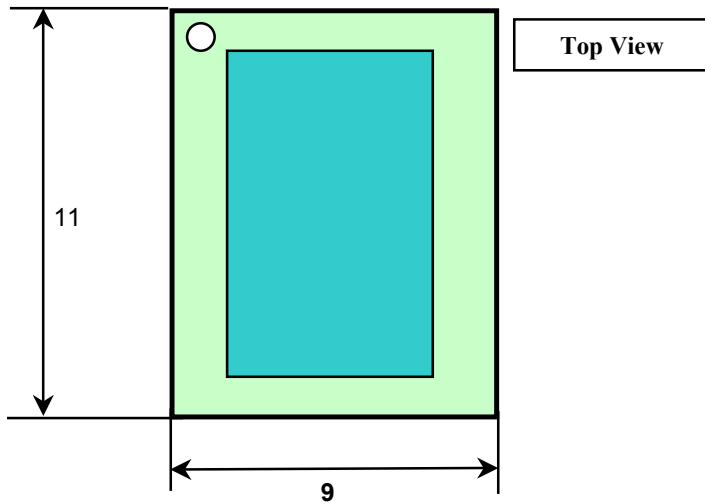
Figure 3. Read mode (1) operation

Next Add. Input

Package Type		TSOP-II 44-P-400-0.8	TSOP-I 48-P-1220-0.50
Top View		<p>Pin connections for TSOP-II 44-P-400-0.8:</p> <ul style="list-style-type: none"> 1: V_{SS} 2: CLE 3: ALE 4: WE 5: WP 18: I/O 1 19: I/O 2 20: I/O 3 21: I/O 4 22: V_{SS} 40: OP 41: R/B 42: RE 43: CE 44: V_{CC} 23: V_{CC} 24: I/O 5 25: I/O 6 26: I/O 7 27: I/O 8 	<p>Pin connections for TSOP-I 48-P-1220-0.50:</p> <ul style="list-style-type: none"> 1: NC 2: NC 3: NC 4: NC 5: NC 6: NC 7: R/B 8: R/B 9: CE 10: NC 11: NC 12: V_{CC} 13: V_{SS} 14: NC 15: NC 16: CLE 17: ALE 18: WE 19: WP 20: NC 21: NC 22: NC 23: NC 24: NC 25: NC 26: NC 27: NC 28: NC 29: I/O 1 30: I/O 2 31: I/O 3 32: I/O 4 33: NC 34: NC 35: NC 36: V_{SS} 37: V_{CC} 38: NC 39: NC 40: I/O 5 41: I/O 6 42: I/O 7 43: I/O 8 44: NC 45: NC 46: NC 47: NC 48: NC
	Package dimensions & Close section View & Memory P/N	<p>Single</p> <p>18.41(L) x 11.76(W) x 1.2 (max) mm</p> <p>64Mbit : TC58V64BFT</p> <p>Stacked</p>	<p>12.0(L) x 20.0(W) x 1.2 (max) mm</p> <p>128Mbit : TC58128AFT 256Mbit : TC58256AFT 512Mbit : TC58512FT</p> <p>12.0(L) x 20.0(W) x 1.2 (max) mm</p> <p>1Gbit : TH58100FT</p>

256M/128M NAND Flash CSP

Package Size	
Design rule	
0.16um	0.13um
256M : 9mm X 11mm	7mm X 10mm
128M : 7mm X 10mm	7mm X 10mm
(7x10 : ● no dummy ball)	



- : Contact Balls
- : Index Mark Ball
- : Dummy Balls

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