

From The Lab to The Fab: Transistors to Integrated Circuits

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Abstract. Transistor action was experimentally observed by John Bardeen and Walter Brattain in n-type polycrystalline germanium on December 16, 1947 (and subsequently polycrystalline silicon) as a result of the judicious placement of gold-plated probe tips in nearby single crystal grains of the polycrystalline material (i.e., the point-contact semiconductor amplifier, often referred to as the point-contact transistor). The device configuration exploited the inversion layer as the channel through which most of the emitted (minority) carriers were transported from the emitter to the collector. The point-contact transistor was manufactured for ten years starting in 1951 by the Western Electric Division of AT&T. The *a priori* tuning of the point-contact transistor parameters, however, was not simple inasmuch as the device was dependent on the detailed surface structure and, therefore, very sensitive to humidity and temperature as well as exhibiting high noise levels. Accordingly, the devices differed significantly in their characteristics and electrical instabilities leading to “burnout” were not uncommon. With the implementation of crystalline semiconductor materials in the early 1950s, however, p-n junction (bulk) transistors began replacing the point-contact transistor, silicon began replacing germanium and the transfer of transistor technology from the lab to the fab accelerated. We shall review the historical route by which single crystalline materials were developed and the accompanying methodologies of transistor fabrication, leading to the onset of the Integrated Circuit (IC) era. Finally, highlights of the early years of the IC era will be reviewed from the 256 bit through the 4M DRAM. Elements of IC scaling and the role of Moore’s Law in setting the parameters by which the IC industry’s growth was monitored will be discussed.

INTRODUCTION

Transistor action was experimentally observed by John Bardeen and Walter Brattain in n-type polycrystalline germanium on December 16, 1947 (and subsequently polycrystalline silicon) as a result of the judicious placement of gold-plated probe tips in nearby single crystal grains of the polycrystalline material (i.e., the point-contact semiconductor amplifier, often referred to as the point-contact transistor) [1-3]. The device configuration exploited the inversion layer as the channel through which most of the emitted (minority) carriers were presumed to be transported from the emitter to the collector. The point-contact transistor was manufactured for ten years starting in 1951 by the Western Electric Division of AT&T [4]. The *a priori* tuning of the point-contact transistor parameters, however, was not simple inasmuch as the device was dependent on the detailed surface structure and, therefore, very sensitive to humidity and temperature as well as exhibiting high noise levels. Accordingly, the devices differed significantly in their characteristics and electrical instabilities leading to “burnout” were not uncommon [5]. With the implementation of single crystalline semiconductor materials in the early 1950s [3,6-8], however, p-n junction (bulk) transistors began

replacing the point-contact transistor, silicon began replacing germanium [5,7,8] and the transfer of transistor technology from the lab to the fab accelerated.

We shall briefly review the historical route by which single crystalline materials were developed and the accompanying methodologies of bipolar transistor fabrication (i.e., grown junction, alloy and diffused). The oxide masking and photolithographic technique of Carl Frosch and Link Derick [9,10] and its embodiment in the mesa process, the utilization of the silicon oxide for the passivation of the silicon surface by Mohammed (John) Atalla and colleagues [11] and the development of the planar silicon transistor by Jean Hoerni (i.e., the planar process) [12-15] whereby the SiO₂ masking layer, utilized in the fabrication of diffused silicon transistors, was left in place for the passivation of p-n junctions intersecting the wafer surface set the stage for MOSFET fabrication as well as the utilization of the dielectric layer for supporting metallic conductor overlayers in the integrated circuit (IC) era [16].

The Si-SiO₂ diffusion technology, transferred from AT&T’s Bell Telephone Laboratories (BTL) to Shockley Semiconductor and, therefore, to Fairchild Semiconductor Corporation led to the phenomenon of “Silicon Valley” and the creation of the IC industry.

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Indeed, Gordon Moore has noted "... and you are once again reminded that this is no longer just an industry, but an economic and cultural phenomenon, a crucial force at the heart of the modern world" [17]. The critical role of John Moll's laboratory at BTL in 1954 and the development of the oxidation, diffusion, lithography, aluminum metallization and thermocompression bonding techniques for the fabrication of the junction transistors and silicon-controlled rectifier [18-21], in conjunction with Nick Holonyak [22], are reviewed.

The oxidation kinetics of silicon by Bruce Deal and Andy Grove [23], the explication of the charge and drift mechanisms in the Si-SiO₂ system by Deal et al. [24-30] and the role of Pieter Balk [31,32] in emphasizing the importance of subsequent hydrogen and nitrogen annealing are briefly discussed. The mesa and planar processes described above paved the way for the invention of the IC by Jack Kilby in 1958 [33-36] (utilizing the mesa methodology in germanium) and Bob Noyce in 1959 [37-39] (utilizing the planar procedure, i.e., in silicon) and the subsequent microprocessor era [40-42]. The critical differences between the two patents (i.e., the interconnection methodology) are clarified by Walter Runyan and Kenneth Bean [43].

The early years of the IC from the 256 bit to the 4 M DRAM are then reviewed [44], building on Bob Dennard's one transistor cell structure [45] and associated scaling methodology [46-49]. Gordon Moore's remarkably prescient assessment that the number of memory bits would double per year (now taken as about 18 months), enshrined as Moore's law, became the productivity criterion by which the IC industry grew at about a 25% compound annual growth rate [50-54] as illustrated in the International Technology Roadmap for Semiconductors (ITRS) [55]. More than just monitoring productivity, whether by staying on the productivity curve or increasing manufacturing effectiveness, however, is required. Rather, modeling productivity—the identification of new productivity measures—is now required [56].

Finally, potential directions for enhanced IC performance, per the ITRS [55], are briefly discussed. These include both carrier transport mechanisms in the channel using variously strained structures to enhance the carrier mobility and new MOSFET device configurations, including various vertical transistor configurations [57].

Single-Crystal Growth

Polycrystalline germanium and silicon were the basic materials used at BTL and elsewhere for transistor research and development in the late 1940's inasmuch as the utilization of single crystals of germanium and

silicon for the transistor was a very controversial matter at that time, although the importance of high-purity material to achieve a high rectification characteristic was understood. Gordon Teal has noted [58]:

"Bill Shockley was opposed to the work on germanium single crystals when I suggested it, because, as he has publicly stated on several important occasions, he thought that transistor science could be elicited from small specimens of polycrystalline masses of material."

Teal, however, was a proponent of the criticality of single-crystal materials for the electronics era, recognizing that Shockley's bipolar junction transistor characteristics [59-62] in single-crystal germanium [63-66] and silicon [67,68] would be substantially better and more reproducible than those of polycrystalline material [6-8,58]. The limited capability for the fabrication of single crystal materials further exacerbated the situation. Indeed, Shockley later realized the shortcomings in his previous assessment of the usefulness and necessity of single crystals [69,70].

Teal believed the fundamental property of a crystalline semiconductor, which would result in its technological importance, was the easily controllable and spatially variable concentration, type and mobility of free carriers, which was indeed found to be the case [71-78]. According to Teal [6-8,58,79-81]:

"I reasoned that polycrystalline germanium, with its variations in resistivity and its randomly occurring grain boundaries, twins and crystal defects that acted as uncontrolled resistances, electron or hole emitters and traps would affect transistor operation in uncontrolled ways. Additionally, it seemed to me that use of this material to produce many complex units meant to be identical, with close performance tolerances, would be inconsistent with high yields and, therefore, also with low costs. Even in developing complex transistor devices, it seemed to me essential to have a high-perfection, high-purity controlled composition semiconductor in order to achieve a separation of various available electron and hole conduction processes in order to analyze and understand the operation of these devices and thus to finally achieve an optimum functional use of them.

My general aims for the single crystal research were as follows: (1) to produce a conducting medium in which a high degree of lattice perfection, of uniformity of structure and of chemical purity is attained; and (2) to build

into this highly perfect medium in a controlled way the required resistivities and electrical boundaries to give a variety of device possibilities by control of the chemical composition (i.e., donor and acceptor concentration) along the direction of single crystal growth.”

The successful initial results obtained in a joint program between Teal and John Little, begun in September 1948, resulted in several germanium rods with some large single crystals in them by pulling from a melt [63,79-81]. The technique employed a single-crystal seed (oriented in a $\langle 111 \rangle$ or $\langle 100 \rangle$ direction), seed rotation and precise temperature control of the melt-solid interface from which the crystal was pulled [6,82-84] (see Figure 1) [84]. These were vital factors in the attainment of single crystals in which the essential semiconducting properties became highly controlled. The method is variously referred to as pulling, the Teal-Little process [63,82] or, somewhat inappropriately, as the Czochralski (CZ) process. Generally, it is simply called the CZ technique, after Czochralski who in 1918 withdrew thin single-crystal metal filaments from a melt [85]. Czochralski did not use a single-crystal seed, however, and apparently did not recognize the significance of directly controlling the melt temperature to control the

crystal diameter. Furthermore, it was noted by Teal in 1952 that in his zeal to develop a single crystal transistor in 1950 [79,80,86]:

“A variety of methods has been employed by various experimentalists to produce single crystals of metals, salts, insulators, and semiconductors. It will be apparent from the scientific literature and the description that follows that the pulling method of growing single crystals of germanium differs materially from the pulling methods of Czochralski, Kyropoulos, Gomerz, Hoyem and Tyndall, and others. There are differences in the materials, designs, and operation of the crystal batch growing equipment. Also, novel techniques were developed to produce germanium single crystals in which the impurity composition and lattice perfection are controlled throughout the crystal. The use of a pulling method for germanium and the employment of new techniques to be described have been vital factors in the attainment of single-crystal in which the essential semiconducting properties are highly controlled.”

In retrospect, it should be noted that during the 1940's the concept, let alone the necessity and usefulness of single crystal materials, was not

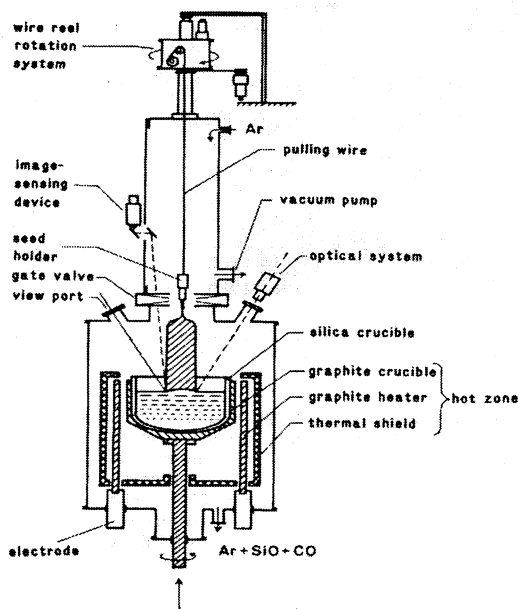


Figure 1. Schematic illustration of a typical Czochralski puller with hot zone, automatic optical and image sensing diameter controls and wire reeling system [84]. Reprinted with permission from Elsevier Science.

appreciated for semiconductor applications. Teal's emphasis on the preparation and characterization of single crystal material, however, facilitated experimental verification of a number of quantum theoretical concepts developed for electrons and holes in crystalline semiconductors such as effective mass, drift and conductivity mobility, carrier lifetime and tunneling [6,58] and clarification of a number of phenomena in p-n junctions [87] and, indeed, exhibited significantly improved characteristics compared to polycrystalline samples. For example, Haynes observed in early 1949 that the lifetime of minority carriers in single crystals of germanium was as much as 140 μ s (20 to 300 times greater than observed in polycrystalline germanium) and mobilities three to four times higher, due to the greater perfection and purity (45 ohm-cm) of the single crystals [6,58,88-90]. Teal also reported injected carrier lifetimes greater than 200 μ s in single crystal germanium as compared to significantly lower carrier lifetimes of 1-5 μ s in polycrystalline germanium [58]. By the early 1950's, all investigators of the semiconducting properties and p-n junction studies of germanium [63-66] and silicon [6,67,68,91,92] preferred to use pulled single crystals. Teal filed for a p-n junction patent in single crystal germanium in 1950 [93] and the first bipolar junction transistor (n-p-n) was achieved in single crystal germanium (grown-junction technique) by Shockley, Morgan Sparks and Teal in 1951 [66], three years after the discovery of transistor action by Bardeen and Brattain [1,2].

The conversion of germanium and silicon ores to metallurgical grade material and their subsequent purification during the 1940's has been reviewed by Frederick Seitz and colleagues [6,94-96]. Seitz also initiated and was the co-editor of the venerable *Solid State Physics – Advances in Research and Applications* series [97], servicing the needs of the physics community from 1955 onwards. Norman G. Einspruch later initiated and was the editor of the invaluable *VLSI Electronics Microstructure Science* series servicing the IC community [98].

Although Teal did not receive the acclaim accorded Bardeen, Brattain and Shockley, his pioneering research and implementation of single-crystal silicon technology as the basis of the IC microelectronics revolution can hardly be over-estimated [7,69,99-101]. The description of dopant distribution during single-crystal growth by normal freezing (see equation 1) was described by William Pfann, via the related zone-refining techniques [102-104], where $C_s(g)$ is the dopant concentration at the fraction of crystal solidified, g , C_i is the initial concentration of dopant in the liquid, d_l and d_s are the

density of the solid and liquid phases, respectively, and k_e , the effective distribution coefficient, is the ratio of the solute concentration in the crystal adjacent to the melt-crystal interface relative to the concentration in the bulk liquid [102-104]. The relationship between the effective distribution coefficient, k_e , and the equilibrium distribution coefficient, k_o , during CZ crystal growth with the crystal growth rate, f (later recognized to be the microscopic crystal growth rate by Kenji Morizane in conjunction with Gus Witt and Harry Gatos [105]; the stagnant boundary layer thickness, δ , at the melt-crystal interface; and the bulk melt flow conditions influencing the solute diffusion coefficient, D , was described by the Burton-Prim-Slichter theory as described in equation 2 [106,107]. This equation was instrumental in conjunction with equation 1, in facilitating the availability of single crystals of germanium and silicon with a specific distribution of dopant impurity [7,63,79,80,82,108] to be discussed below. An extensive summary of the equilibrium distribution coefficients and solubilities for a variety of elements in crystalline germanium and silicon were summarized by Forrest Trumbore [109].

$$C_s(g) = k_e C_i (1 - g)^{k_e(d_l/d_s) - 1} \quad (1)$$

$$k_e = k_o [k_o + (1 - k_o) \exp(-f \delta/D)]^{-1} \quad (2)$$

The role of microscopic fluctuations in the dopant distribution, both radially and axially along the crystal, were to have profound implications on device performance to this day [8]. Pfann and colleagues initiated methodologies to rectify this situation [110].

Finally, a rather innocuous observation that silicon crystals grown by the CZ method contain parts per million atomic (ppma) concentrations of oxygen [111-113] (due to the dissolution of the quartz crucible by the molten silicon), and has had extremely important repercussions to the present day [114,115]. The higher melting point of silicon at 1420°C, compared to germanium at 937°C, resulted in contamination using the previous, conventional graphite containers. This contamination was overcome by utilizing fused quartz crucibles to hold the liquid silicon rather than graphite, with the unintended consequence that the melt became saturated with oxygen. This topic and methodologies for the localized removal of the oxygen from the near-surface regions of the fabricated device and its utilization as effective internal gettering bulk sites has been extensively discussed [7,8,115,116] and will not be further discussed in this review.

Bipolar Transistor Fabrication

Grown-Junction Bipolar Transistors

The path by which the role of group III and V impurities were deduced as p- and n-type dopants, respectively, in silicon and the critical role of metallurgy was reviewed by Jack Scaff [117,118]. The n- and p-type impurity dopants such as phosphorus and boron, respectively, were shown by Greiner's x-ray studies of the variation of the lattice constant with dopant concentration to occupy substitutional sites in the group-IVa semiconductors such as germanium and silicon, as reported in [71]. The inference was that all group III and group V dopants behaved in this manner in germanium and silicon [117]. The ground states are typically 40-50 meV from the appropriate band edge for silicon [6,119,120] (donors below the conduction-band edge, acceptors above the valence-band edge) and are readily ionized at 300K where the number of free carriers is essentially equal to the dopant density as determined by neutron activation analysis (NAA) [121].

The deduction of the role of group III and V impurities as p- and n-type dopants, respectively, in germanium, in conjunction with equations (1) and (2), led to the first grown junction n-p-n transistors, based on the "double-doping" technique in 1951 [64]. Since it was easier at the time to make good contact to a p-type base in an n-p-n transistor rather than to an n-type base in a p-n-p transistor, the former became commercially available, subsequently followed by the p-n-p transistor using a more complicated process [122]. Pellets of gallium and antimony alloys of germanium were sequentially (and rapidly) added to the melt during the growth of an n-type germanium crystal [64]. Only one slice of n-p-n germanium junction transistors, however, could be fabricated by this technique, which was subsequently superseded by Robert Hall's "rate-growth" technique, introduced in 1952 [123-125]. This technique is based on the variation of the incorporation of acceptor or donor impurities into the solidifying germanium semiconductor with the crystal growth rate. A series of germanium regions containing numerous p-n junctions (obtained by slicing the crystal) were grown within the same crystal [123] and n-p-n transistors with good yields and performance at intermediate radio frequencies were also achieved [124,125]. Further extension of the utilization of two different impurities in various structures within the same germanium crystal were carried out by Hall [123-125] as well as by Bridgers and Kolb [126,127].

With the subsequent development of the microwatt junction transistor in germanium [66], the benefits of larger current handling capability and less noise in the junction, compared to the point-contact, transistor [5] led to the escalation of the former,

especially after improved techniques to control the base width—and thus increase the frequency response, an initial limitation [128]—were subsequently developed [129]. Specialized techniques to improve the point-contact transistor characteristics of germanium, however, such as the gold bonded diode [99] continued. Nevertheless, small-area silicon diodes replaced germanium point-contact diodes by about 1960. The silicon devices, first reported in 1952 by Gerald Pearson in conjunction with Sawyer and Philip Foy utilized the alloying technique (see below) to fabricate silicon diode rectifiers via an aluminum doped (p-type) wire alloyed to an n-type Si material that could operate up to 300°C [130,131]. It was clear, however, that the future was with the silicon bipolar junction transistor [129], which itself became eclipsed with the advent of the silicon MOSFET in the 1970's.

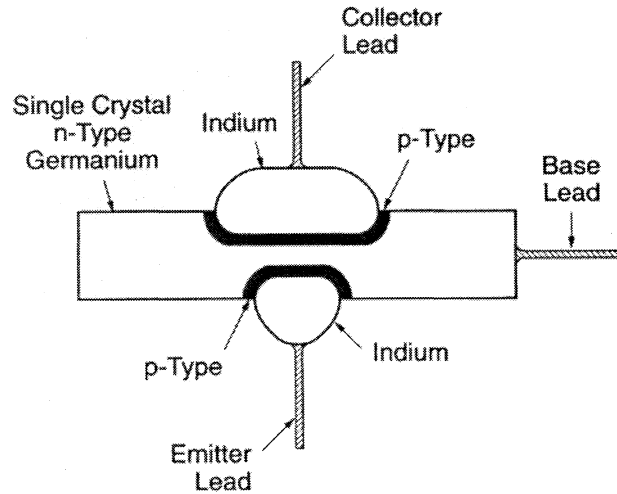
A commercially feasible grown-junction silicon transistor, introduced by Teal in 1954 [132], was subsequently described by Willis Adcock, in conjunction with Mort Jones and colleagues [133], although an experimental silicon transistor was previously announced in 1950 by BTL [134]. The silicon transistor raised the power output and doubled the maximum operating temperature previously attained by germanium transistors. These results clearly demonstrated that silicon was superior for transistor performance compared to germanium and vastly expanded the types of applications for which transistors could be used [6]. Morris Tannenbaum and co-workers subsequently reported that additions of gallium and antimony dopants supported the growth of single crystals of silicon containing up to five n-p-n regions of grown junction silicon transistors [135]. Junction transistors were cut from the slices and the base layer was located and contacted, which was not a trivial process.

Alloy Bipolar Transistors

Concurrently, John Saby developed the alloy transistor in 1952 [136] as did J. Trevor Law and colleagues [137], building on Hall's research [138,139]. The alloy process has been described, in retrospect, as crystal dissolution and regrowth or local liquid phase epitaxy (LPE) on both surfaces of silicon or germanium [22]. For example, arrays of indium dots were positioned on opposite surfaces of an n-type slice of germanium cut from a CZ grown germanium crystal (see Figure 2 for a schematic illustration of a p-n-p transistor) [4]. Alloying was accomplished, on individual die, in an inert atmosphere of about 600°C, during which the recrystallized germanium incorporated some of the indium, thereby converting to p-type. The achievement of a precise and narrow base width,

however, by controlling the alloying temperature was difficult and the achievement of very high cut-off frequency performance was also quite difficult [22].

interface to expose the {111} surface orientation during alloying [18]. This resulted in the decision to utilize that surface plane for device fabrication



p-n-p Alloyed Germanium Junction Transistor

Figure 2. Schematic illustration of the alloy transistor [4]. Reproduced by permission of the IEEE, Inc.

For example, the maximum cut-off frequency of an alloy germanium p-n-p transistor was typically 10 MHz [140] while a germanium point-contact transistor exhibited typical values up to 50 MHz [141]. The fabrication problems were exacerbated inasmuch as the emitter-base junction and the collector-base junction were fabricated from opposite surfaces of the n-type and p-type silicon or germanium slice for p-n-p and n-p-n transistor fabrication, respectively [22]. The viability of achieving a controlled base width for a silicon n-p-n alloy transistor was quite difficult due to the variability of the process [22]. Nevertheless, alloying (because of its presumed simplicity) was readily implemented as a manufacturable process and became widely utilized (compared to the more uncontrollable base widths for grown-junction devices) for transistors in germanium [137,142] and silicon for many years [4], although the silicon alloy transistor was very difficult to fabricate and never commanded a significant market position [43].

The challenge of upgrading to the GHz range was a goal, required to support the extensive range of anticipated electronic applications. Since, as noted earlier, it was easier at the time to make good contact to a p-type base in an n-p-n transistor rather than to an n-type base in a p-n-p transistor [122], the latter did not become prominent in the marketplace. Finally, it should be noted that there was a strong preference of the melt-crystal

to enhance the ability to form a uniform alloy; this choice of surface orientation was to continue throughout the bipolar junction and bipolar IC era. The onset of the MOS era in 1968, however, quickly shifted focus to the {100} orientation, which exhibited a reduced concentration of interface states at the Si-SiO₂ interface and facilitated better control of the MOS threshold voltage [24,143-145] as well as was advantageous for III-V devices (i.e., lasers).

There is a fundamental difference in the emitter-base and base-collector junctions between the alloy and grown-junction transistors. The alloy junctions are abrupt (of the "step" type) while the grown-junctions are graded. Accordingly, the alloy transistor exhibited a higher alpha cut-off frequency range (5-10 MHz) than the grown-junction transistor (1-10 MHz) due to the emitter-base step junction, although the abrupt base-collector junction for the alloy transistor resulted in a higher capacitance per unit area, tending to limit the high-frequency response. An alternate method of transistor fabrication, referred to as a surface barrier alloy transistor [146], was able to achieve cut-off frequencies up to 50 MHz by utilizing an electrochemical fabrication technique [147]. The approach was pioneered by Philco, using a jet etching technique, in which the germanium is etched by an electronically controlled jet of electrolyte [146]. Subsequent alloy contacts on each side of the thinned

base material resulted in a higher cut-off frequency, due to the factor ten smaller base width, compared to the grown-junction transistor. The mechanical fragility and low production yield, however, precluded the surface barrier transistor from becoming more widely disseminated. Concurrently, although the cut-off frequency of the point-contact germanium transistor had approached 50 MHz [147], it was the grown-junction and alloy junction devices, which continued to be produced on a mass-production basis into the late 1960's [43,147]. Likewise, the micro-alloy diffused transistor [148] received some attention, but was soon eclipsed by the introduction of the diffused mesa and planar transistor due to their lower leakage current and greater mechanical stability as described below.

Diffused Bipolar Transistors

The double-doping and rate-growth techniques were critical to proving out the junction transistor theory in practice. There were, however, inherent limitations in their manufacture as regards their commercial applicability. The junctions, for example, were physically inside the crystal and the p-type base layer was thicker and less uniform than desired. The introduction of solid-state diffusion procedures, with a key patent issued to Scaff and Henry Theuerer in 1951 (filed in 1947) [149] and implemented by Pearson and Calvin Fuller [150] rectified this situation via the in-diffusion of impurities in a controlled ambient over the whole slice of the semiconductor. The technique involved the exposure of the semiconductor slice to a vapor, containing the dopant of sufficient concentration, in a carrier gas to ensure the controlled dopant concentration at the semiconductor surface and at a sufficiently high temperature to create diffusion rates that would provide precise control of the dopant penetration depth in the semiconductor. Diffused layers from a few tenths of a μm to 20 μm were achieved. The initial study of the diffusion of donors and acceptors in germanium was published by Fuller [151] followed by Fuller and Ditzenberger's research of diffusion in silicon [152]. The silicon diffused junction rectifier was described by Prince in 1956 with peak reverse voltages of 400 V and current ratings of 400 mA [153]. By the mid 1950s, improvements in semiconductor processing facilitated the fabrication of both n-p-n and p-n-p transistor structures by solid-state diffusion processes in a mesa structure (see Figure 3) [4]. Lee fabricated a p-n-p germanium mesa transistor in 1954 with a base width of 1.0 μm by a diffused arsenic base and alloyed Al emitter; the current amplification factor

and cut-off frequency were 0.98 and 500 MHz, respectively [154]. By 1959, germanium mesa transistors were being fabricated with base widths of 0.2 μm and, in the early sixties, silicon with cut-off frequencies approaching 1000 MHz were fabricated in double-diffused planar epitaxial structures (see below) [155]. Tannenbaum and Thomas fabricated a diffused base and emitter n-p-n mesa Si transistor with a base width of 2 μm , in 1956, with a current amplification factor and cut-off frequency of 0.97 and 120 MHz, respectively [156]. Tannenbaum and Thomas's work is of especial importance in that it utilized the simultaneous diffusion of both the acceptor (for the base) and donor (for the emitter) dopants, albeit their concentrations were appropriately different to ensure the desired transistor action. Friedolf Smits reviewed the spectrum of solid-state diffusion techniques now available [157].

Mesa and Planar Processes

The mesa process was described by Aschner et al. in 1959 [158], who noted it was essential that the emitter diffusion proceed more rapidly than the base diffusion to retain control of the base width while the oxide masking and photolithographic technique, pioneered by Frosch and Derick [9,10] to be discussed below, was also utilized to remove a portion of the top of the semiconductor slice, resulting in the characteristic mesa structure. This geometrical modification was essential in order to reduce the p-n junction area so as to reduce the depletion layer capacitance and achieve the desired high frequency characteristic. Utilization of the diffusion (mesa) process, furthermore, opened the pathway for the fabrication of devices slightly below the planar surface of the semiconductor wafer, with far-reaching implications. These included narrow, well-controlled base widths, about a factor ten smaller than for the grown-junction and alloy transistors [159], and, thereby, higher frequency operation. Many transistors could be made at one time on each slice of Si or Ge during the "batch" processing with rather similar characteristics, especially important for adjacent devices with matched device characteristics for high-performance circuit applications, and many slices were available from each CZ grown crystal. Mesa transistors fabricated by the oxide masking and photolithographic technique were less expensive to fabricate compared to grown-junction transistors or alloy transistors, although all these fabrication methods, to some extent, were prone to excessive leakage currents. The initiation of the concept of the "learning curve," based on the reduction in the cost of

producing numerous identical devices through the cumulative process experience, was enunciated by Patrick Haggerty with implications to the present day [160-162].

With the advent of the diffusion process, the device frequency limitation was transferred from the base to the collector region [4]. It appeared that there was a basic, built-in design conflict inasmuch as the diffusion process resulted in the collector having the highest resistivity, compared to the emitter and base. Ross noted that “this led to significant series resistance in the collector, and that, combined with the capacitance of the collector junction, limited the frequency response” [4]. While the collector resistivity could be reduced, this resulted in a higher capacitance and lower breakdown voltage at the base-collector junction inasmuch as the base had to be highly doped to minimize the base resistance and small width to reduce the transit time. Jim Early had previously (before the introduction of the diffused transistor) proposed a device design solution by the

suggesting a cut-off frequency as high as 3000 MHz. The state-of-the-art cut-off frequency in 1954 of 95 MHz was realized for a p-n-i-p germanium transistor proposed by Early [163]. Ross noted that Early “had the distinction of being the only person other than Shockley to propose a basically new transistor structure” [4], although one may regard the innovation more of a design modification. The fabrication of such a structure, however, required the diffusion or alloy process to be incorporated from both surfaces of the semiconductor slice, thereby resurrecting the experimental problem of accurate control of the base width. Nevertheless, Early significantly improved the understanding of the static characteristics of conventional bipolar transistors by also utilizing a heavily doped, thin base such that the space-charge widening in the collector (due to the reverse bias at the collector-base junction) enhanced the bipolar transistor’s transit time [164,165]. This also had the effect of causing a portion of the depletion region to spread onto the base side of the

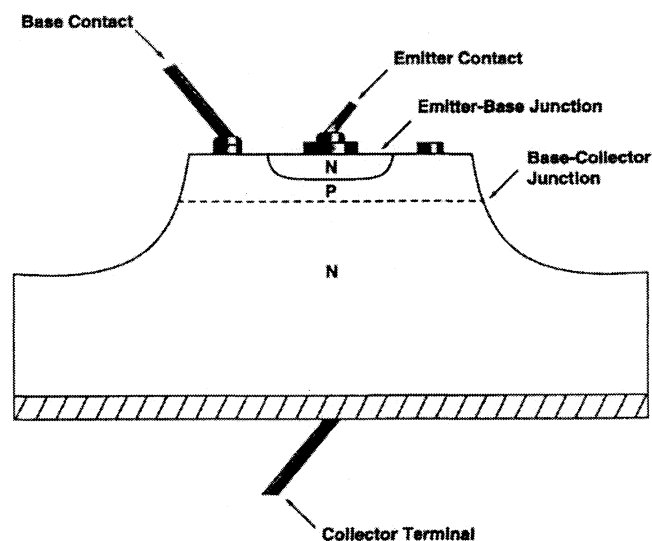


Figure 3. Schematic cross-section of an early mesa transistor made by Fairchild Semiconductor Corporation [122]. Reproduced by permission of the IEEE, Inc.

introduction of an intrinsic or very high resistivity layer between the base and the collector to create a p-n-i-p structure [163]. This allowed an increased collector doping while retaining a low capacitance and high breakdown voltage of the collector since, under a reverse bias, the space charge region would penetrate the total width of the intrinsic region,

junction (even though the base was more highly doped than the collector), thereby reducing, somewhat, the effective base width for the transport of minority carriers to the collector. This resulted in an increase of the current gain factor (α) and a decrease in the emitter potential required to ensure a given emitter current [164,165].

The solution to achieving the p-n-i-p or n-p-i-n structure was obtained by the fabrication of a lightly doped layer of silicon on a heavily doped silicon substrate, referred to as epitaxial fabrication [166-169]. Henry Theurer and colleagues [169] expanded the applicability of epitaxial structures by implementing Bernard Murphy's localized, high-concentration sub-collector diffusion in a lightly doped silicon substrate [170-172], before epitaxial deposition, which enhanced bipolar performance by reduced collector resistance. The development of high-frequency, small signal devices via the newly developed planar process (see the *Planar Process* section below) was, however, limited to reverse junction breakdown voltages of only a few hundred volts and, since the junction area was small, to limited power handling capabilities. As a result, the development of high-power, high-voltage

furthermore, was silicon's oxide, SiO₂, which was insoluble in water, whereas germanium's oxide was water soluble [3,7]. This attribute of silicon facilitated its utilization in the planar process as a diffusion mask for p-n junction fabrication as developed by Frosch and Derrick [9,10], the fabrication of the planar silicon transistor by Hoerni [12-15], passivation of the silicon surface and p-n junctions intersecting the surface by Atalla and colleagues [11] and a dielectric layer for supporting metallic conductor overlayers in the IC era [16]. Indeed, with the advent of the planar process, increased breakdown voltage behavior along with reduced reverse leakage current was achieved [175].

All the elements were now available (oxidation, diffusion, photolithography, aluminum metallization and thermocompression bonding [4,7,20-22]) for the

Table 1. Technology Evolution For Controlled Base Width Transistors

Technology	Author	Approximate Year	Reference
Double-doping	Teal	1951	64
Rate-grown	Hall	1952	123-125
Alloy	Hall	1950	138,139
Electrochemical thinned base	Tiley and Williams	1953	146
Diffused base	Pearson and Fuller	1954	150
P-N-I-P (N-P-I-N)	Early	1954	163
Planar process	Hoerni	1960	12
Epitaxy	Teal, Sangster, Mark, Theurer	1954, 1957-1960	166-169

rectifiers and transistors with reverse junction breakdown voltages of several thousand volts as well as thyristors continued to proceed via utilization of the mesa process, although there was, naturally, strong interaction between these two complementary approaches (i.e., mesa and planar) so that the separation was not as sharp as might be indicated. Table 1 broadly summarizes the evolving technological trends to control the base width for junction transistors.

As noted earlier, silicon rapidly replaced germanium for transistor fabrication [6-8,16,43] as a result of silicon's larger energy gap which facilitated higher-temperature device operation and lower reverse current, effective four-layer n-p-n-p or p-n-p-n switching devices [19,173,174] as well as the plentiful availability of single crystals with the requisite purity, perfection and controlled electrical properties [6-8,86,119]. Germanium was relegated as a niche material for specialty devices, such as low-power, requiring performance metrics not readily achievable with silicon. Of especial importance,

fabrication of junction transistors and the silicon controlled rectifier (SCR) (also referred to as the four-layer switch or thrysistor), in Moll's laboratory [18,21], in conjunction with Holonyak [22]. The SCR, developed by Moll in conjunction with Holonyak and colleagues, has a rich history [19,20,22,163,174].

The state of device physics had now reached a sufficiently sophisticated level that Holonyak relates that "Moll asked Holonyak, in conjunction with LeLacheur's familiarity with the systems requirements on switching transistors, to prepare a preliminary design "theory" to permit all of our colleagues to become familiar with what could be expected of the new silicon transistors" [22,176]. Inasmuch as this internal BTL memorandum [176] was not subsequently published, an excerpt is noted below [22].

"Some of the design variables of diffused impurity transistors are discussed. Design compromises between series collector

resistance and collector capacity are found to be necessary. The relative advantages of linear and circular structures are considered both for base resistance and for collector capacity. Parameters, which are expected to affect the frequency behavior, are considered, including emitter depletion layer capacity, collector depletion layer capacity and diffusion transit time. Finally the parameters which might be obtainable are compared with those needed for a few typical switching applications."

The Planar Process

The development of oxide masking by Frosch and Derick [9,10] on silicon deserves special attention inasmuch as they anticipated planar, oxide-protected device processing. Silicon is the key ingredient and its oxide paved the way for MOSFET integrated electronics [22]. An account of their revolutionary development and utilization of SiO₂ as the vital foundation of today's IC industry has been described by Holonyak [22]:

"In building our various experimental devices, we were in contact with various groups and individuals, but above all with Carl Frosch. Frosch was a consummate process chemist who was familiar with many types of processing procedures and had been working, with his technician Derick, on impurity diffusion into silicon for several years. In spite of his considerable experience, Frosch, with dry gas diffusion procedures utilizing N₂ or H₂, regularly reduced many of our silicon wafers to "cinders," particularly at higher temperatures ($\geq 1100^\circ\text{C}$).

Because we had mastered building a diffused-base alloyed-emitter silicon p-n-p transistor (in spite of our problems with diffusion), one of the p-n-p-n configurations that we could explore was simply a modification of the p-n-p transistor: We could fabricate the diffused-base alloyed-emitter p-n-p on one side of a p-type substrate wafer after it first was prepared with an n-type diffused region (symmetrical) on both sides of the wafer. Either side could be chosen to form the p-n-p. The result was a p-n-p-n switch, in fact, the p-n-p-n switch of example (b) as described in [19]. (The complementary version of this exact structure, an n-p-n-p with Ga diffused into both sides of an n-type silicon wafer and then a Au-Sb emitter alloyed on one side, was later introduced at General Electric as the first

commercial silicon controlled rectifier, today's thyristor. This later work was also based on our 1956 research [19].

In the process of diffusing the p-type substrate wafer into an n-p-n configuration for the first stage of p-n-p-n construction, particularly in the redistribution "drive-in" phase of the donor diffusion at higher temperature in a dry gas ambient (typically $\geq 1100^\circ\text{C}$ in H₂), Frosch would seriously damage our wafers. The wafer surface would be eroded and pitted, or even totally destroyed. Every time this happened the loss was apparent by the expression on Frosch's face, not to mention, on ours (N.H.). We would make some adjustments, get more silicon wafers ready, and try again.

In the early Spring of 1955, Frosch commented to Holonyak, "Well we did it again," meaning the wafers were again destroyed. But then he smiled and displayed the silicon wafers – nice and green in color (in further instances also pink). He and his technician Derick had switched from a dry-gas (typically N₂ or H₂) impurity diffusion to a wet-ambient (H₂O vapor + carrier gas) diffusion, a consequence of an accident of the exhaust H₂ igniting and flashing-back into the diffusion chamber (because of gas flow fluctuations) and causing H₂O to cover, react with, and protect the silicon samples with oxide. The "wet" ambient, which was then immediately evaluated and adopted, created a protective oxide on silicon. It could be selectively removed for gaseous diffusion into the bare regions, which could then be resealed with oxide for higher temperature anneals or further diffusion. Many processing sequences could be devised for use of the protective oxide, which, of course, prevented crystal pitting and erosion. Frosch and Derick quickly found out which impurities were blocked from diffusion into silicon by the natural protective oxide (SiO₂) created in an H₂O-vapor ambient and which impurities would permeate the oxide (e.g., Ga). It was easy, once the issue of the oxide was known, to devise various schemes to diffuse into or to block impurity diffusion into silicon. The process was so flexible that planar n-type regions of any desired pattern could be prepared on a p-type substrate silicon, or the opposite, p-on-n diffused regions could be prepared on n-type silicon. All other diffusion procedures were suddenly rendered obsolete. We readily converted the Frosch-diffused silicon n-p-n into a working p-n-p-n switch [19]."

Holonyak [22] noted “what Frosch and Derick had done was to set the basis for a revolution. In fact, it is the oxide on silicon that is the basis, the vital foundation of today's IC chip, and of all of the silicon devices so critical to the electronics industry. Because of our (Holonyak) exploratory silicon device work and our involvement with Frosch, we were close observers and witnesses of his work. For example, on p.15 of an extensive BTL memorandum [177], Frosch wrote:”

“Thin silicon slices also were diffused with Sb for N. Holonyak for preliminary device development investigations. These were diffused for 2, 5 and 16 hours respectively at 1300°C in N₂ saturated with water vapor at room temperature. After diffusion, these slices were green in color with an excellent surface appearance. These layers were reported to have resistivities of from 10 to 20 ohms per square. The diffusion layers were reported to be uniform in thickness being 0.26, 0.39 and 0.76 mils respectively for the 3 heating times. An additional run was made for Holonyak to produce layers of somewhat higher resistivity. In this run the thin silicon slices were heated for 1 hour at 1200°C followed by 16 hours at 1300°C in N₂ saturated with water vapor at room temperature. These samples again were green in color with excellent surface appearance. These were reported to have resistivities of 45 to 90 ohms per square with a diffusion depth of 0.66 mils. The higher resistivity values obtained indicate not only a lower solubility of the Sb compound in the quartz envelope at 1200°C than at 1300°C but also the essential absence of Sb compound vapor in the carrier gas when the temperature was raised to 1300°C. Holonyak was able to produce very promising cross-point switches from some of these Sb diffusions.”

Holonyak [22] continues by saying “we knew Frosch's work at first hand, and realized immediately what he and Derick had done. All of us near this work, which was just a few at first, realized its importance, but, in truth, none of us, least of all Frosch, in his exceeding modesty, projected it to its true future scale. Frosch even wrote (p. 20) the following statement in his BTL memorandum [177]:”

“In addition to the possibilities of process simplification, the protective quartz envelope

added during the heating may be useful for protecting an electrical device from atmospheric conditions. For example, the device might prove more stable if left enclosed in such a quartz envelope. However, it may not be possible to make all of the necessary electrical contacts through the quartz. In these cases some protection may be retained by the removal of a small area of the envelope for the application of the contacts.”

Holonyak has summarized Frosch's innovation by “Frosch had, indeed, anticipated planar, oxide-protected device processing. He appreciated immediately the importance of the oxide. It is questionable if anyone else's contribution had as much to do with the existence of the “chip” and today's electronics as Frosch's oxide. This is easily seen by simply raising the question: *Remove the oxide, say it doesn't exist, and then what would there be? Silicon itself is, of course, the critical ingredient followed by its unique natural oxide. In some sense it could be said that Si and its technology (its oxide) “invented” the IC,*” (italics entered by the author).

The benefits of SiO₂ on the surface properties of silicon were concurrently, or shortly thereafter, assessed by Attala's group [11,178]. They believed that growing an oxide under clean and controlled conditions, on a properly cleaned silicon wafer, would lead to both a reduction of surface states and passivation of the silicon surface. The planar diffused transistor developed by Hoerni [12-15] of Fairchild Semiconductor Corporation in the late 1950's pulled together a number of these strands as regards the benefits of SiO₂ and was in production by 1959. These included the concept that the SiO₂ masking layer, utilized in the fabrication of diffused silicon transistors, be left in place for the passivation of p-n junctions intersecting the surface in the case of the grown junction, alloy and diffused mesa transistors, without the necessity of growing a passivating oxide under meticulously clean conditions [179], per the insight of Hoerni [12-15] as well as ensuring a dielectric layer for supporting metallic conductor overlayers in the IC era [16]. The Si-SiO₂ diffusion technology had, in point of fact, been transferred from BTL to Shockley Semiconductor, to Fairchild Semiconductor Corporation and, from there led to the creation of Silicon Valley [180]. Numerous testimonies as to the efficacy of the planar approach have been presented [122,158,181]. Sparkes noted [159]:

“Victor Grinich of the Fairchild Corporation presented graphs of the change with time of current gain, base-emitter voltage and cut-off current of planar transistors which were so much better than anyone had seen before that it was quite obvious that if they were genuine a real breakthrough had been achieved. After several hours’ discussion with Grinich it became clear to me that the planar process was the process of the future. It was an unpalatable conclusion, since, just at that time, many companies had recently invested large sums of money in the double-diffused, the alloy-diffused or micro-diffused process with the hope of achieving a clear production run of a few years.”

To more fully appreciate the significance of passivating the p-n junction intersecting the surface in the mesa transistor such as fabricated by AT&T, one may consider Moore’s assessment [122]:

“In mesa transistors, the emitter-base junction is exposed on the top surface between the metal contacts, while the base-collector junction intersects the sides of the mesa (see Figure 3). The regions of high electric fields where the junction comes to the surface are sensitive to contamination. Contamination of the emitter-base junction can decrease the gain of the transistor dramatically. In the case of the collector junction, the breakdown voltage and leakage characteristics can change. We noted a problem that some of the transistors packaged in hermetically sealed cans in dry nitrogen showed very unstable collector junction characteristics. Breakdown voltages sometimes decreased by several tens of volts and became unstable when observed on an oscilloscope, potentially a major reliability problem. We formed a task force to try to understand and correct the problem. One of our technicians, B. Robson, carefully cut the can off one of the bad devices and examined it under a microscope. He noticed a spot of light emitted from the side of the mesa when the transistor was biased into breakdown. He shut off the power and saw a tiny particle on the side to the mesa at the point of the light emission. Carefully removing the particle and reapplying power, he found that the original high breakdown voltage was restored. The particle, evidently attracted by

the high electrical field where the junction came to the surface, was causing the premature breakdown of the junction. Now we knew the cause of the low breakdown. All we had to do was eliminate all the sources of particles.”

The planar process introduced extreme flexibility in the fabrication of junction transistors, since the “tooling up” to fabricate different devices involved changing the mask set, diffusion profiles and doping levels and, as appropriate, the resistivity of the starting material. The planar process additionally facilitated the fabrication of a double-diffused transistor essentially planar with the original wafer surface, without the necessity of a mesa structure. A photomicrograph of the first planar transistor is shown in Figure 4 [122]. Chin-Tang (Tom) Sah, Harry Sello and Tremere published the first quantitative analysis of the oxide masking thickness and related time and temperature processing to ensure blockage of the diffusing impurity in the oxide masked region [182]. It was especially important that these planar transistors had the base contact completely surrounding the emitter so as to eliminate any chance of the base inverting, as was the case for the original bipolar junction transistors [183,184]. With the advent of the planar technique, cut off frequencies in the range of 10 GHz could now be achieved, approaching values achieved for vacuum tubes [185]. Indeed, the exodus of Bob Noyce, Gordon Moore, Jean Hoerni, Jay Last, Julius Blank, Victor Grinich, Eugene Kleiner and Sheldon Roberts 1957 from Shockley Semiconductor Laboratory, established in 1955 [69,122], and their subsequent formation of Fairchild Semiconductor Corporation with the stated goal of fabricating double-diffused transistors for commercial gain (the original goal of Shockley Semiconductor before Shockley redirected its effort to the p-n-p-n diode [174]) was the major stimulus to the invention of the planar transistor, Silicon Valley and the development of the fledgling electronics industry. On the other hand, it should be noted that Shockley, Noyce, Moore et al. were cognizant of developments at BTL as regards SiO₂ and were quite receptive to its advantages in the fabrication of silicon junction transistors. In fact, the entire diffusion technology at BTL was made available to Shockley to help facilitate his ambition to derive a measure of success in the business world based on the transistor technology he had helped to develop. Shockley was not, however, to achieve his business goals but contributed, inadvertently, to the exodus from Shockley Semiconductor which, in conjunction with Stanford University’s graduates, led

to the Silicon Valley phenomenon. Indeed, Shockley has been referred to as the “Moses of Silicon Valley” [186].

established the basis for the utilization of the aluminum metallization system [22]:

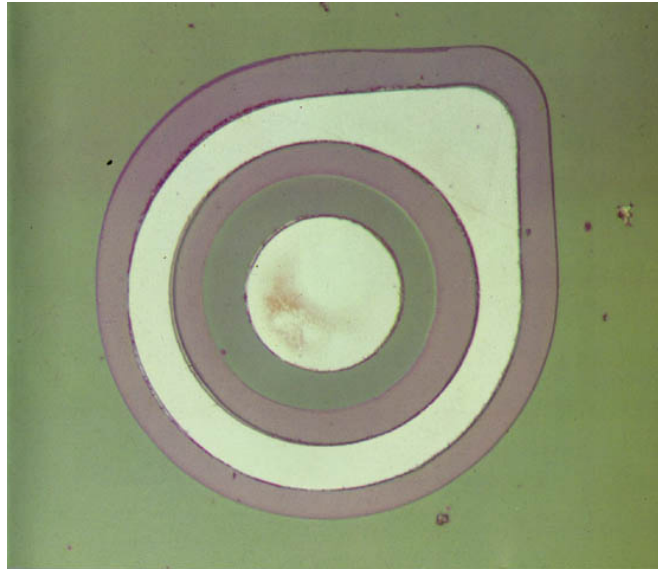


Figure 4. Photomicrograph of the first planar transistor. The diameter of the circle that forms most of the outside ring is 0.030 in. The light areas are aluminum emitter and base electrodes. (From “A Solid State of Progress,” Fairchild Camera and Instrument Corporation, 1979) [122]. Reproduced by permission of the IEEE, Inc.

As noted earlier, the critical elements for the fabrication of the transistor and thyristor and, subsequently, the IC electronics era (oxidation, diffusion, photolithography, aluminum metallization and thermocompression bonding) were now all available. Jules Andrus and Bond showed that certain photoresists, when deposited on SiO_2 , would protect the underlying SiO_2 during etching processes [180,187,188]. Optical exposure of the resist using contact masks in the late 1960's and early 1970's, projection masks in the middle 1970's and stepper mask methodologies beginning in the later 1980's was used to create precise window patterns (open regions) in the oxide and, therefore, precise control of diffusion areas. Aluminum metallization was utilized to form ohmic contacts to both p- and n-type material. While the former was expected due to Al being a group III dopant, the latter was achieved since the contact was subsequently identified to form a tunnel diode with the n-type silicon, the tunnel diode characteristic being linear (and, therefore, simulating an ohmic contact) for both small positive and negative voltages about the origin. Moore and Noyce received a patent for the aluminum metallization [189]. Holonyak has described the experiments conducted at BTL which

“Satisfactory Al evaporation on Si did not exist when our work started. Moll obtained permission from Tanenbaum for us to use his evaporator, and we quickly solved the problem of evaporating Al on Si, on “hot” or on “cold” Si, and were able to realize precise shallow alloyed p-type contacts or shallow “p” on “n” p-n junctions. We were able to show the various conditions under which uniform evaporated Al contacts could be realized on Si: (1) If the Si substrate was 660°C or hotter, the evaporated Al (mobile Al) nucleated at random sites that grew into larger diameter islands with more evaporated Al, and formed a discontinuous regrown region. (2) In the temperature range between the Al-Si eutectic (577°C) and the melting point of Al (660°C), uniform sticking and wetting of the Al occurred and formed continuous metallized and alloyed-regrown p-type Si without further heating. (This was nothing more than Hall's “local” liquid phase epitaxy LPE [139,140]. (3) For the Si substrate at temperature 577°C or lower, the evaporated Al merely adhered (uniformly) on the Si, and subsequently could be alloyed or could be left as a Schottky barrier. By late 1954, Goldey and Holonyak had solved the problem of metallizing Si and

forming uniform shallow p-n (or n-p) junctions, or if desired, shallow ohmic contacts. Holonyak soon wrote a BTL memorandum on Al metallization and shallow junction formation on Si [190] and Goldey incorporated this material and some further results in a report published later [191].”

Contacts from the junction transistor to the header were usually made by thermocompression bonding, developed at BTL by O.L. Anderson, H. Cristensen and P. Andreasch [4]. Typically, gold (melting point 1063°C) was brought in contact with the aluminum bonding pad (melting point 660°C) in a reducing atmosphere under pressure. The gold-aluminum eutectic formed at about 350°C which, upon cooling, formed a strong, reliable bond. It was subsequently observed that a phenomenon referred to as “purple plague” often developed due to undesired reactions between the gold wires and the aluminum bonding pads at the upper range of temperatures where silicon transistors operate. The aluminum and gold formed a series of colored intermetallics (i.e., the purple plague) that ultimately caused device failure [43]. Rectification of this yield degradation was subsequently achieved by restricting the temperature range of operation (also required for the plastic packages then utilized), utilization of all aluminum systems using aluminum leads, wires and aluminum coated package connections [43]. Gold metallization systems such as the beam lead method [192] and multilevel metallization schemes [193,194] were also developed.

The benefits of the planar research in conjunction with Hoerni’s insights resulted in the first meaningful description of the MOSFET device

(formation of an inversion layer, i.e., enhancement mode) by Dawon (David) Kahng and Attala in 1960 [195-198], also summarized by Sah [44]. Kahng wrote an extensive BTL technical memorandum on the silicon/silicon dioxide device in 1961 [199]. Steven Hofstein and Frederick Heiman of the Radio Corporation of America (RCA) followed with an MOS IC consisting of 16 silicon n-channel MOS transistors in 1963 [200]. It should also be noted that J. Torkel Wallmark of RCA took out a patent on an FET in 1957 [201] but apparently did no further work in the field while Paul Weimer constructed an FET using CdS as the dielectric material on an insulating substrate in 1959 [202]. Although these structures were minority-carrier devices, the Metal-Semiconductor Field Effect Transistor (MESFET) and the Junction Gate Field Effect Transistor, see Figure 5 [4], first described and patented by Shockley [203,204] and built by George Dacey and Ian Ross [205] were majority carrier devices [44,206,207].

MOSFET Transistor Fabrication

The description of the oxidation process and methodologies for controlling the electrical properties of the silicon/silicon dioxide interface in the late 1950’s were essential for the successful commercialization of the MOSFET and implementation of the DRAM memory era in the 1970’s (see the *Integrated Circuit* section.) Deal and Grove described the oxidation kinetics of silicon [23], followed by Dennis Hess [208], Eugene Irene [209], Hisham Massoud [210] and Stanley Raider [211] and their colleagues who extended this research. Richard Williams [212] and Akos Revesz [213] also made

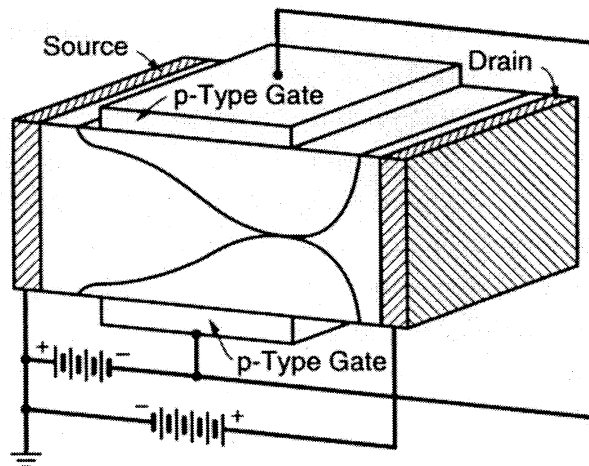


Figure 5. Schematic of the junction field-effect transistor [4]. Reproduced by permission of the IEEE, Inc.

significant contributions to the understanding of the silicon/silicon dioxide interface while George Schnable [214] advanced our understanding of a host of dielectric film deposition methodologies for Integrated Circuit (IC) applications [8].

Device reliability studies by Ed Snow, Grove, Deal and Sah at Fairchild Semiconductor identified that sodium contamination in SiO₂, introduced by the heated tungsten filament [215] for aluminum evaporation, was mobile under voltage stress, caused device parameters to drift under operating bias and was exacerbated by increased operating temperature. The Fairchild team also observed that electron-beam evaporation did not introduce the sodium [215], thereby developing techniques for controlling the sodium and, furthermore, developed an extensive understanding of the phenomena taking place in the metal-oxide-silicon system that is basic to all modern MOSFET systems. Deal described the silicon/silicon dioxide electrical interface stability and associated effects in silicon dioxide in terms of 17 types of charge mechanisms and introduced the standard description for the charge notation associated with thermally oxidized silicon [24-30]. The reduction of mobile charges, fixed charge (Q_f) and interface state charge (D_{it}) as well as the control of the growth process (oxide thickness) was of paramount importance in ensuring threshold voltage control and the successful commercialization of MOS device products [216]. While most of the industry initially chose to fabricate PMOS devices, some companies elected to fabricate NMOS because of the higher channel mobility for electrons, compared to holes. However, positive charge control is a more serious issue in NMOS technology. Post-oxidation and post-metallization anneals were developed in the 1960's to minimize both fixed and interface charge [31,32]. The mobile charge, such as Na and K, also required stringent control.

Techniques were developed for the passivation of surface states introduced at the silicon/silicon dioxide interface during thermal processing. Pieter Balk described in 1965 the significance of a post SiO₂ anneal in a hydrogen bearing ambient [31] and a nitrogen anneal in the case of the Al-SiO₂-Si system [32] to stabilize the Si-SiO₂ interface and reduce the fixed charge, Q_f. Molecular hydrogen was suggested to anneal the surface states by bonding with the dangling silicon and oxygen bonds [31,32]. Kooi of Philips Research Labs in Eindhoven confirmed Balk's research [217]. Sah has noted that Balk's hydrogen annealing methodology has withstood the test of time for more than 30 years and is a fundamental aspect of the MOSFET IC processing methodology [44]. Sah has quoted from Balk's

abstract [31] (Sah's comments are added in curly brackets):

“The main effect of the H₂ treatment appears to be the annihilation of fast states {another name for interface states}. If these states are related to vacancies, accompanied by chemically unsaturated bonds {has been known as dangling bonds} and unpaired electrons near the interface, the H₂ {not hydrogen ion or proton as some think} annealing may be in effect the chemical saturation {now known as hydrogenation} with H atoms of these bonds at the vacancies. The low state density obtained upon steam oxidation is probably caused by hydrogen, evolved during oxidation, and retained in the oxide. The similarity in action between H₂ and Al remains as yet unexplained.”

Balk clarified the unresolved issue as regards the similar benefit between a H₂ and an N₂ anneal of Al later that year in 1965 [32]. Sah [44] again quotes Balk:

“The similarity of the annealing behavior of the electrical interface properties of Si-SiO₂ in H₂ and Al-SiO₂-Si in N₂ around 300°C suggests that the same mechanism is operative in both cases. Hydrogen released in a reaction between Al and hydroxyl groups in the oxide is proposed as the active agent in the Al-SiO₂-Si case. This model is supported by the absence of any annealing effects on ‘ultra-dry’ oxide.”

It was suggested that residual H₂O, released from the Al during thermal processing, reacts with the hydroxyl groups to yield hydrogen. Sah further points out the beneficial effect of annealing in H₂ or forming gas (95% N₂/5% H₂) [218]:

“Balk's hydrogen bond model of passivating and deactivating the interface traps has also been the chemical-atomic base for the characterization of the generation, annealing and charging kinetics of the interface and oxide traps due to silicon and oxygen dangling bonds.”

Balk's insight was extremely important during the early 1970's, when Al was still the dominant gate electrode, before the introduction of the polysilicon gate electrode and the fabrication of the 1K and, in some cases, the 4K dynamic random access memory (DRAM)

IC. The last thermal process step (before packaging) was a 30 minute or so anneal between 400°C or 450°C to ensure sufficient reaction of the aluminum with the silicon for good contacts; the release of H₂ from the aluminum during the 450° C anneal was instrumental in passivating the interface states and recovering the desired threshold voltage. The role of hydrogen annealing and passivation in the broader context of the plasma deposited overlayer of silicon oxynitride as a seal over the entire circuit has also been discussed [219].

Dalton and Dorbek of AT&T [220] demonstrated that an overlayer of Si₃N₄ could also provide an effective seal against sodium ions; to avoid the concurrent trapping of hydrogen ions resulting in threshold voltage instabilities, silicon oxynitride was subsequently utilized. Indeed, a plasma deposited overlayer of silicon oxynitride is used as a seal over the entire circuit structure, except for the contact pads [4]. The nitride film is also very effective in reducing pinholes in the SiO₂ dielectric. Concurrently, Kerr and Don Young of IBM were developing the utilization of a phosphosilicate glass (PSG) deposited on top of the MOS gate dielectric silicon dioxide to getter the Na and K and stabilize the oxide film [221,222]. This approach was especially important for aluminum gate electrodes, utilized prior to the phosphorus doped polysilicon gate technology to be discussed below. Snow and Deal [223], followed by Pieter Balk and Jerome Eldridge [224], showed that the threshold voltage shifts of MOSFET's, induced by polarization in the PSG layer on the SiO₂ surface, could indeed be controlled. Stabilization of the surface was also beneficial for bipolar transistors for operation at low currents or high voltages where deterioration of the current gain and leakage current due to surface instabilities degraded device performance and yield.

Concurrently, Rudolf Kriegler championed an in-situ furnace gettering methodology in the early 1970's, to remove sodium as well as other deleterious contaminants such as metals and transport these mobile ions and lifetime-killing metallic impurities from the wafer to the gaseous ambient. This procedure became an especially prevalent industrial technique [225-227]. Typically, about 3% gaseous HCl or Cl₂ in the O₂ oxidation ambient [227] was utilized, similar to Robinson and Heiman [228]. Carl Osburn studied the improvement of gate oxide integrity (GOI) via these Cl methodologies [229] as part of an extensive series of analyses in the Very Large Scale Integration (VLSI) laboratory of Arnold Reisman [230]. TCE (trichloroethylene) [231] and TCA (trichloroethane) [232] were subsequently utilized with similar benefits, but without the

corrosive effect of the HCl ambient on the furnace metal plumbing.

Gettering was initially believed to occur by formation of volatile metal chlorides, although the Gibbs free energy of formation of most metal chlorides was not negative. The Cl, however, was also interpreted as removing interstitials, as evidenced by the shrinkage of oxidation induced stacking faults (OISF) at sufficiently high temperature by Hiromitsu Shiraki [233], Cor Claeys [234] and their colleagues. Shih-Ming (Jimmy) Hu showed that the shrinkage (retrograde growth) of OISF at sufficiently high temperatures in the absence of HCl was dependent on both the surface orientation and ambient [235]. The early utilization of these Cl ambients was in conjunction with the oxidation ambient during high-temperature processing. The Cl incorporated in the SiO₂ also trapped and immobilized the sodium at room temperature. It was suggested by Kreigler and Osburn, furthermore, that it might be more advantageous to clean the furnace quartz tube in the presence of the Cl bearing species but not to incorporate the Cl into the SiO₂ film, per se, due to SiO₂ reliability considerations [227,229].

The subsequent capacitance-voltage (C-V) diagnostic analysis of the Si-SiO₂ interface electrical properties by Moll [236] and Terman [237], was expanded upon by Grove, Snow, Deal and Sah [238] and formulated in a set of useful charts for fabrication engineers by Zaininger and Heiman [239]. Edward Nicollian and Adolf Goetzberger's conductance analysis [240-243] quantified the description of the silicon/silicon dioxide interface electrical properties while the p-n junction under non-equilibrium conditions was described by Grove and Fitzgerald [244]. The description of oxidation kinetics by Deal and Grove [23] and the local oxidation of silicon (LOCOS) process developed by Kooi and colleagues in the late 1960's [245-247], which was instrumental in the fabrication and achievement of superior MOS IC characteristics (see Figure 6) [247], set the stage for the initiation of the MOSFET Dynamic Random Access Memory (DRAM) era in the early 1970's. The LOCOS process has been the mainstay for CMOS IC fabrication for more than 30 years and only now is shallow trench isolation seriously challenging its utilization [248].

The mesa and planar processes described above now paved the way for the fabrication of the IC by Jack Kilby (utilizing the mesa methodology) [8,33-36,43] and Robert Noyce [8,37-39,43] (utilizing the planar procedure), in 1958 (see *Integrated Circuit Beginnings* section) and, subsequently, the microprocessor [40-42].

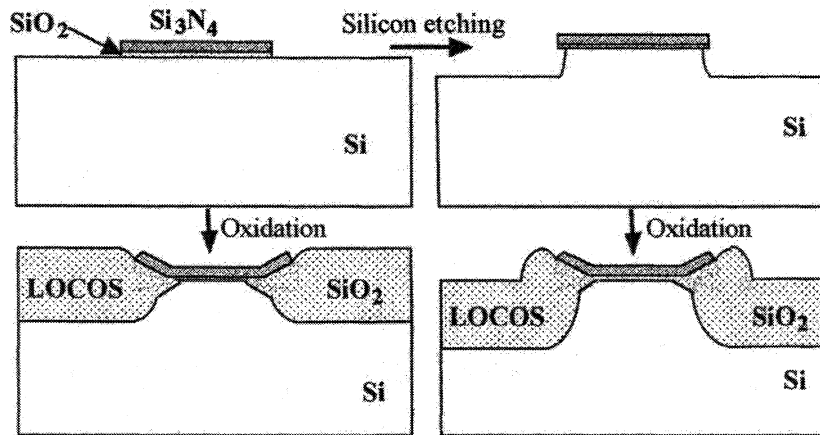


Figure 6. Conventional LOCOS procedures. A pad oxide (SiO_2) under the nitride oxidation mask relieves stress, but results in the formation of “bird’s beaks” at the oxide edges. Fully recessed oxide patterns (right) exhibits complete “bird’s heads” [247]. Reproduced by permission of The Electrochemical Society, Inc.

Integrated Circuit Beginnings

The challenge after implementation of the junction transistor era in the 1950s was to not only emulate the vacuum tube in as many applications as possible (without the excessive power generation and reduced operating lifetime), but to exploit the inherent advantages of solid-state electronics to new arenas. The smaller device dimensions required to achieve higher frequency operation in the junction transistor was confronted, however, with the inherent challenge of the limited power-handling capability due to the device’s small size. The goal of achieving higher operating frequency and higher power-handling capability seemed to be at odds with each other. Ross described the situation as follows [4]:

“In the meeting on that day, we were, as was frequently the case, discussing our problems in emulating the vacuum tube. R. Wallace suddenly said:

“Gentlemen, you’ve got it all wrong! The advantage of the transistor is that it is inherently a small size and low power device. This means that you can pack a large number of them in a small space without excessive heat generation and achieve low propagation delays. And that’s what we need for logic applications. The significance of the transistor is not that it can replace the tube but that it can do things that the vacuum tube could never do!”

“And this was a revelation to us all. We realized that in chasing the vacuum tube, we had the wrong emphasis.... The net result was that the semiconductor community began to relax about replacing the tube and focused on developing the transistor in its own right. The transistor did eventually replace the tube in all but a few special applications, the magnetron being one outstanding example. But it took decades. In the meantime, semiconductor technology opened up important new fields that the tube could never have supported.... Having the clear goal of an application for an invention is a powerful stimulus for innovation. But frequently, the original application turns out not to be the most important.”

In a similar vein, Robert Lucky has recently noted “moreover there is no *a priori* way to determine what will tip a market. It’s a fundamental instance of chaos in-group dynamics. And that makes it fundamentally difficult to predict future societal behaviors in the adoption of technologies [249].”

Until the invention of the IC, electronic systems were comprised by individually connecting the various components (vacuum tubes or transistors, diodes, capacitors, resistors and inductors) together. The common feature of these endeavors was the wiring together of discrete and separately packaged device components. Of course, it was essential that these components be spaced sufficiently close so that the system propagation delay did not become the factor limiting the system speed. This required the

miniaturization of the system, not just the device components. Two major system concerns surfaced which required rectification. This involved the assembly yield and reliability of a system with thousands of device components, which might be unacceptably low. Additionally, even if the device components had no errors, there would be a multitude of connections, resulting in the infamous “tyranny of numbers” [35,36,250-253].

Lester Hogan reviewed what may be the earliest attempts to rectify the “tyranny of numbers” conundrum [254]; that is, the patents filed by both Darlington [255] and Oliver [256] in 1952. Darlington and, apparently, Oliver used a grown junction transistor; both patents integrated several transistors on one piece of germanium or silicon, although they included no passive components. Geoffrey Dummer of the Royal Radar Establishment (RRE) at Malvern, England initiated his solution to the integration challenge in 1952 [257] and subsequently described his work at the Malvern Components Symposium in 1957 [258] and elsewhere [259]. Runyan and Bean [43] have quoted Dummer’s 1952 status as “an integrated approach using a monolithic block comprising” [258,259]:

“...layers of insulating, conducting, rectifying and amplifying materials, the electrical functions being connected directly by cutting out areas of the various layers.”

Hogan [254] has also quoted a portion of Dummer’s presentation at the 1957 meeting [258]:

“... a transistor flip-flop with two emitter follower outputs—a total of four transistors all contained in a chip of silicon 125 mils by 375 mils. The semiconductor was doped to form a p-n-p structure and had various sections removed to leave thin bridges of material with relatively high resistances. These high-resistance paths formed the collector and emitter loads of the transistors connected to common power supply rails. Other resistors were provided by films of resistive material deposited on the surface of the silicon, while capacitors were constructed from thin metallic layers with insulators between.”

Concurrently, Harwick Johnson of RCA was also developing his solution to the integration challenge [260]. Hogan [254] described Johnson’s contribution:

“As early as 1953, Harwick Johnson of RCA conceived of a complete phase shift oscillator

built in a single chip of n-type germanium where p-n junctions supplied the necessary capacitance, the body resistance of the piece of germanium supplied the resistive elements and an alloy transistor at one end of the filamentary piece of germanium supplied the necessary amplification.”

“The significant point is that only two years after the first junction transistor was reported [reference added [66], research people were already trying to combine resistors, capacitors, (diodes) and transistors into one piece of semiconductor material in order to reduce size, to reduce the number of interconnects and to improve reliability.”

The alloy junction transistors utilized by Johnson as well as the other, multi-faceted, approaches by personnel familiar with the state-of-the-art in the attempts to build an integrated circuit in the mid 1950’s was perhaps best described by Dummer to be “pioneering stages” ... not capable of production [261].” Dummer’s review of the work in Great Britain and Western Europe is also of interest [262].

Runyan and Bean [43] have commented about Johnson’s contribution:

“The figures included in a patent ... by Harwick Johnson ... (reference [260] added) bear a superficial resemblance to an integrated circuit. However, as expressed in the first sentence of the patent, both the discussion and claims relate only to a transistor phase-shift oscillator: ‘This invention pertains to semiconductor devices and particularly to semiconductor phase-shift oscillators and devices.’ Component isolation was not considered so that even if the concepts of the patent were extended to devices other than the phase-shift oscillator, the class of devices that could be made would be very limited.”

It was Kilby of Texas Instruments, Incorporated, however, who filed a patent application on February 6, 1959 [8,33-36,43] explicitly “describing a concept that allowed, using relatively simple steps, the fabrication of all the necessary components of the desired circuit, both active and passive, in a single piece of semiconductor and their interconnection in situ” [43]. Kilby’s initial proof of concept was a phase shift oscillator, built with about ten components, in germanium for expediency [43] on September 12, 1958. Wire bonding was utilized to

interconnect the components within the chip (see Figure 7).

material, the junctions of such components being near and/or extending to one face of the body,

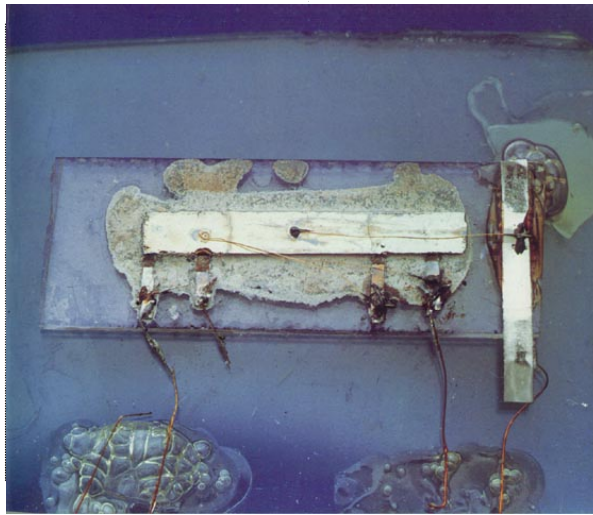


Figure 7. The first integrated circuit, a phase shift oscillator fabricated in germanium by the mesa process, invented by Jack S. Kilby of Texas Instruments in 1958, courtesy of Texas Instruments Incorporated.

A few weeks later, a flip-flop circuit was made and a patent application covering both germanium and silicon was prepared and filed (February 6, 1959). The first commercially available IC, intended for binary counter, flip-flop or shift register applications, was fabricated in silicon and announced in March, 1960 by Texas Instruments. Runyan and Bean [43] have extracted several relevant portions of Kilby's patent [33], with appropriate commentary:

"In contrast to the approaches to miniaturization that have been made in the past, the present invention has resulted from a new and totally different concept for miniaturization.... In accordance with the principles of the invention, the ultimate in circuit miniaturization is attained using only one material for all circuit elements and a limited number of compatible processing steps for the production thereof.... "

Up to this point, the goals are perhaps not much different from those expressed in 1952 by Dummer. However, to continue with the Kilby patent:

"In a more specific conception of the invention, all components of an electric circuit are formed in or near one surface of a relatively thin semiconductor wafer characterized by a diffused p-n junction or junctions...."

"It is a primary object of the invention to provide a miniaturized electronic circuit wherein the active and passive circuit components are integrated within a body of semiconductor

with components spaced or electrically separated from one another as necessary in the circuit...."

"Figures 1-5a (in reference 33 added by author) illustrate schematically various circuit components fabricated in accordance with the principles of the present invention in order that they may be integrated into, or as they constitute parts of, a single body of semiconductor material:"

Runyan and Bean [43] continue, "The figures and text describe bulk resistors, diffused resistors, pn junction capacitors, MOS capacitors, transistors, and diodes. In the press coverage of the March 1959 announcement of the Kilby concept, this set of standard components was stressed [263]. The patent text continues:"

"Because all of the circuit designs described above can be formed from a single material, a semiconductor, it is possible by physical and electrical shaping to integrate all of them into a single crystal semiconductor wafer containing a diffused p-n junction, or junctions, and to process the wafer to provide the proper circuit and the correct component values...."

With the subsequent planar process patent submission by Hoerni of Fairchild Semiconductor Corporation on May 1, 1959 [15] and due to manner in which the interconnection was described in Kilby's patent [33] compared to Noyce's IC patent application, filed on July 30, 1959 [37], Noyce was actually awarded

a patent before Kilby's (April 25, 1961 compared to June 23, 1964). Figure 8 is a photomicrograph of one of the first planar integrated circuits made at Fairchild Semiconductor Corporation [122]; subsequent evolutionary trends have been

then referencing the relevant portion of the Noyce claims [37]:

"... an electrical connection to one of said contacts comprising a conductor adherent to

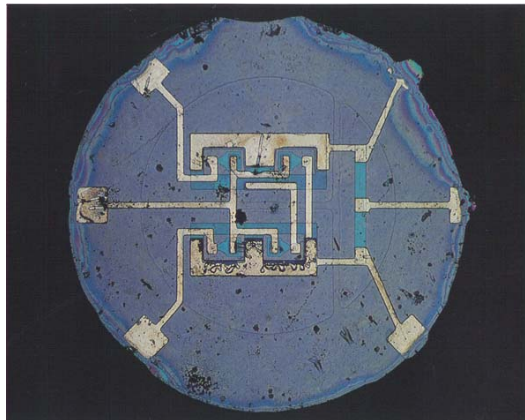


Figure 8. Photomicrograph of one of the first planar integrated circuits made at Fairchild (in silicon). This is a flip-flop circuit (with two transistors). Some of the aluminum interconnection metal has been damaged during the etching operation to form a circular chip of silicon to place into a transistor can modified to have more leads. (From "A Solid State of Progress," Fairchild Camera and Instrument Corporation, 1979) [122]. Reproduced by permission of the IEEE.

described for ICs [44]. The Texas Instruments IC was developed utilizing the mesa process while Intel utilized the subsequent planar process. The legal battle that ensued between Texas Instruments and Fairchild Semiconductor centered around the wording associated with the interconnection scheme. Runyan and Bean [43] have summarized the essence of the point of contention between the Kilby and Noyce patent dispute, quoting Kilby's patent [33]:

"Instead of using the gold wires 70 in making electrical connections, connections may be provided in other ways. For example, an insulating and inert material such as silicon oxide may be evaporated onto the semiconductor circuit wafer through a mask either to cover the wafer completely except at the points where electrical contact is to be made thereto, or to cover only selected portions joining the points to be electrically connected. Electrically conducting material such as gold may then be *laid down* (italics entered by author) on the insulating material to make the necessary electrical connections."

said layer (italics entered by author)" The disagreement centered around whether "*laid down*" was equivalent to "adherent to." The Board of Patent Interference, ruling in Kilby's favor, asserted that it was. However, a subsequent ruling by the Court of Customs and Patent Appeals (*Noyce v. Kilby*; *Kilby v. Noyce*, decided November 6, 1969) reversed the previous rulings and allowed the Noyce claims. (The Supreme Court then refused to review the case.) Contrary to assertions by some, the ruling did not depend on whether gold could or could not be made suitably adherent to silicon oxide. The Court specifically commented on that aspect. The ruling depended on the Court's assessment of whether or not someone reading Kilby's statement would be inevitably drawn to the conclusion that the lead should be adherent."

Runyan and Bean then continue [43]:

"Probably the most balanced assessment of Kilby's and Noyce's relative contributions is contained in the citations of the Franklin Institute's 1966 Ballantine Medal award, which they shared. Kilby was credited for 'conceiving and constructing the first working monolithic circuit in 1958,' and Noyce for 'his sophistication

of the monolithic circuit for more specialized use, particularly in industry.’ ”

Implementation of the IC concept was somewhat slow in consideration of the anticipated yield of an IC containing, say, 100-1000, transistors. That is, the reliability of a chip was anticipated to approximate the reliability of a discrete transistor degraded by a power to the number of transistors or components [4,264]. It turned out, however, that neither the yield or reliability was determined by random events degrading the transistor uniformity, per se, due to the batch method of silicon IC processing [4]. In point of fact, there tended to be large areas of a silicon wafer where the yield was close to 100% while the yield in other areas tended to zero [265]. Thus, if the IC chip area was small compared to the area on the wafer with high yielding ICs, the yield would be essentially independent of the chip size and the number of chips per wafer. With this realization, the stage was set for the IC explosion. Ross [4] has quoted Kilby in discussing the buildup of IC production [34].

“It should be noted that one of the great strengths of the integrated circuit concept has always been that it could draw on the mainstream efforts of the semiconductor industry. It was not necessary to develop crystal growing or diffusion processes to build the first circuits, and new techniques such as epitaxy would be readily adapted to integrated circuit fabrication. Similarly, new devices such as MOS transistors and Schottky barrier diodes would be phased in as they became available. Even today, it is difficult to identify a process that is used only for integrated circuits.

Another strength of the concept was that it could draw on existing circuit technology to produce a broad range of useful devices....

Because of the commonality with existing processes, integrated circuits moved rapidly into a production status.”

It might be appropriate, however, to note that developments in IC fabrication to enhance device performance and scaling have significantly expanded the spectrum of processes uniquely developed for IC

fabrication, including, for example, self-aligned structures and the lightly doped drain (LDD) configuration (see Integrated Circuit Scaling section).

While the use of epitaxy had been an important design consideration for discrete transistors, its real impact occurred with the introduction of the bipolar IC. Prior to epitaxy, component isolation within the bipolar IC was achieved by reverse-biased p-n junction isolation techniques (introduced by Lehovec on April 22, 1959 [266,267]) such as by diffusion (consider boron) from both the front- and back-surfaces of the wafer until the diffusion fronts met in the center of the n-type wafer, leaving n-type wells in the masked regions. Runyan and Bean have reviewed the p-n junction isolation technique, including Lehovec’s contribution to the interconnection methodology as well as the isolation techniques utilized by Kilby and Noyce [43]. Kenneth Bean has also described his epoch research on dielectric isolation for Bipolar ICs with Paul Gleim and Runyan [268,269]. The advent of epitaxial structures, however, offered a new design flexibility in component isolation. For example, one could utilize a thin n-type epitaxial layer (say 3 μm , for example) on a p-type substrate wafer. Component isolation could readily be achieved by boron diffusion through the epitaxial layer. Additionally, the fabrication of structures with a high concentration of dopant in the collector, to decrease transistor collector resistance, was achieved by the localized diffusion of an n-type dopant into a p-type substrate wafer prior to the growth of an n-type epitaxial layer [166-169].

Integrated Circuit Fabrication

Although the bipolar transistor exhibited better performance characteristics such as switching speed than the MOSFET transistor, the process simplicity and smaller IC chip size of the latter made it the preferred choice for implementation of leading edge design rule applications [270-272]. The first mass produced commercial MOS DRAM design was Intel’s 3-transistor silicon-gate PMOS, 1K DRAM announced in 1970. Terman [273] and Hodges [274] have reviewed a number of these memory developments prior to 1972, often referred to as the small-scale integration (SSI) era (see Table 2 for an approximate taxonomy of the evolving DRAM).

TABLE 2: DRAM Process and IC Evolution (circa 1992)

Parameter	Units	ULSI	VLSI	LSI	MSI
Bits/chip	Number	$10^7 - 10^9$	$10^5 - 10^7$	$10^3 - 10^5$	$10^2 - 10^3$
Design Rule	μm	< 1	1 – 3	3 – 5	5 – 10
Power-delay product	PJ	$< 10^{-2}$	$10^{-2} - 1$	1 – 10	$10 - 10^2$
Mask levels	Number	15 – 20	8 – 15	6 – 10	5 – 6
Chip area ^a	mm^2	50 – 280	25 – 50	10 – 25	10
Storage cell capacitor equivalent oxide thickness	(nm)	3.5 – 12.5	12.5 – 40	40 – 90	90 – 120
Junction depth	μm	0.04 – 0.2	0.2 – 0.5	0.5 – 1.2	1.2 – 2

a) Chip area (or more specifically, active device area) significantly impacts IC yield in conjunction with the defect density per cm^2 per critical lithographic level (for the number of critical levels).

The transition to the self-aligned aluminum gate and then the self-aligned phosphorus doped polysilicon gate adjacent to the source and drain junctions via ion implantation of the junctions, reducing the Miller capacitance [275-279] and the transition to the silicide metalization scheme [280] were significant achievements enhancing IC performance. An additional device innovation was Heiman's utilization of a four-terminal configuration for the MOSFET by applying a negative dc voltage to the substrate [281] which modified the threshold voltage of the MOSFET (increased the threshold voltage for an n-channel MOSFET) and is referred to as the "body effect." This may be seen in the threshold voltage, V_T , expression in equation 3 for an n-channel transistor (with no ion implant for V_T adjust) [282]:

$$V_T = -\frac{(Q_f/C_{OX})}{N_A} + 2\phi_F + \phi_{MS} + (1/C_{OX}) (2 \epsilon_{Si}\epsilon_0 q) N_A^{1/2} (2\phi_F + V_{BB})^{1/2} \quad (3)$$

where:

Q_f = Fixed positive interface charge per unit area at the silicon-silicon dioxide interface. The positive charge contributes electrons to the p-type silicon at the surface, thereby making it easier to invert the p-type bulk silicon to an n-type surface inversion channel (i.e., lower V_T)

C_{OX} = Gate oxide capacitance per unit area

ϕ_F = Bulk Fermi energy relative to the the intrinsic Fermi energy (for 10^{15} holes/ cm^3 , $\phi_F = -0.29$ V)

ϕ_{MS} = Work function difference between the phosphorus doped polysilicon gate and the p-type silicon substrate (taking the Fermi energy in the phosphorus doped polysilicon at the edge of the conduction band, $\phi_{MS} = -0.84$ V)

ϵ_{Si}/ϵ_0 = Dielectric constants of silicon (11.7) and vacuum, respectively

V_{BB} = Substrate back-gate bias ($V_{BB} = -5$ V for the 4K and 16K DRAM when this technique was popular). Substrate bias also reduces the junction capacitances of the source, drain and channel, an important performance advantage.

The body-effect technique also allowed determination of the bulk substrate doping, N_A , at the edge of the surface space charge region (SSCR) for comparison with that deduced by capacitance-voltage (C-V) analysis via equation 4:

$$N_A = \left[\frac{(C_{OX}) \partial V_T / \partial (2\phi_F + V_{BB})^{1/2}}{(2 \epsilon_{Si}\epsilon_0 q)} \right]^2 \quad (4)$$

Physically, the substrate near the surface is reverse biased by the negative V_{BB} body bias, thereby negating, somewhat, the influence of the electrons donated by the fixed positive charge, Q_f , at the interface and increasing V_T to the desired range. It should be noted that the $2\phi_F$ term does not scale with device scaling.

The larger number of device functions on a given MOSFET IC chip and the larger number of MOSFET IC chips for a given wafer diameter were instrumental in ensuring the eventual dominance of the MOSFET IC. Fairchild announced a 64 bit SRAM (six transistor cell design), enhancement-mode p-channel MOSFET in 1964 [44] followed by RCA's announcement and production of an enhancement mode n-channel MOSFET, also in 1964, based on Hofstein and Heiman's research [283]. Frank Wanlass and Sah of Fairchild Semiconductor Corporation disclosed the Complementary MOS (CMOS) IC in 1963 [284,285] followed by RCA Corporation later in the year [286]. Wanlass's initial demonstration circuit, a two transistor inverter, consumed a few nanowatts of standby power, compared to milliwatts of standby power for equivalent bipolar and PMOS gates [287]. Interestingly, Wanlass utilized Heiman's back-bias methodology [281] to achieve an n-channel enhancement mode device (due to the difficulty of uncontrolled surface charges at that stage of technology to fabricate an n-channel enhancement-mode MOS transistor) to work in conjunction with the conventional PMOS enhancement-mode transistor [287].

CMOS eventually became the ultimate MOSFET technology, since both p-and n-channel enhancement-mode transistors are normally off, drawing only quiescent power; that is, only during the switching process is significant power dissipated [286,288-290]. The DRAM memory array in CMOS ICs was fabricated in NMOS while the peripheral drivers were fabricated in CMOS. U.S. companies tended to use the same design rule for both the NMOS memory array and the CMOS peripheral devices, accentuating the latch-up phenomenon, thereby requiring the use of epitaxial structures to minimize latch-up (the coupling of an n-p-n MOS transistor with an adjacent p-n-p MOS transistor forming an n-p-n-p or p-n-p-n thyrister [289,290]. It appears the Japanese used a larger design rule for the CMOS circuitry, thereby avoiding the use of epitaxial wafers. The Japanese approach was less costly to fabricate since polished, rather than epitaxial, silicon wafers were used. Although there were less chips per wafer due to the larger chip size, increased yields often negated the geometrical limitation. MOSTEK, Incorporated, formed in 1968,

was the first semiconductor company exclusively devoted to the fabrication of MOSFET ICs. Shortly thereafter, the 256 and 1K DRAM MOSFET IC was introduced by Texas Instruments in 1970 and 1972, respectively. Intel introduced the 1K PMOSFET DRAM in 1970 [291]. Indeed, Intel's 1K p-channel (PMOS) DRAM (polysilicon gate), based on a three-transistor cell design, initiated the beginning of the MOS memory take-over of the ferrite core memory market by its implementation at computer maker Honeywell, Inc. [292].

The MOSFET IC revolution, however, really exploded when IBM chose the n-channel silicon MOSFET (NMOS), instead of the slower p-channel silicon MOSFET, for its mainframe memory computer (IBM-370/158) that was delivered in 1973. The access time of the NMOS was in the range of nsec while magnetic core memory's access time was about one μ s. Intel and MOSTEK were early suppliers followed by TI in 1974. TI's design was based on the one-transistor DRAM cell structure of Bob Dennard [45] and described by others [293,294], also summarized by Sah [44]. Texas Instruments and MOSTEK utilized a single-metal-word-line/single-diffused-bit line [44,295-297], where the metal was Al and the source and drain were formed by diffusion. Texas Instruments utilized $POCl_3$ in forming the diffused source and drain. The 4K NMOS DRAM cell built by Intel was a single-poly-word-line/single-metal (Al)-bit line [44,295-297].

The 16K DRAM was announced in 1976, with three significant changes made compared to the 4K DRAM, noted by Sah [44]. These were a reduction of the design rule from the 7-8 μ m regime for the 4K DRAM to about the 5 μ m range for the 16K DRAM; the removal of the source diffusion which became known as the merged one-transistor DRAM cell and an overlapping double polysilicon gate, one for the sourceless transistor (the pass gate) and the second for the charge storage capacitor, thereby forming the merged one-transistor DRAM cell [44,295-297]. The wafer diameter was also subsequently increased to three-inches and, later, changes to larger diameters became commonplace when the number of DRAM chips became less than about 100 per wafer [298]. The subsequent transition to the 64K DRAM around 1979 did not result in any change in the cell design, although the design rule was reduced to the 2-3 μ m range and the part was subsequently implemented on four-inch diameter wafers [298]. Four significant IC process changes were discussed by Sah [44]. These included a parallel plate storage capacitor, rather than storage in a surface inversion layer, to give a higher charge storage capacitance (about 32 fF to store $\approx 10^6$ electrons at 5V V_{DD}) from the small area of the one-

transistor DRAM cell, since higher capacitance was required to reduce the soft errors due to noise electrons generated by alpha particles from the package materials of the chip, cosmic rays and other noise sources [44]; a dual dielectric for the charge storage capacitor, utilizing the higher dielectric constant of silicon nitride formed by chemical vapor deposition (CVD) on thermally grown silicon dioxide to enhance the composite storage medium's dielectric constant and to reduce pinholes in the thinner silicon dioxide (not all DRAM manufacturers utilized this option); plasma etch technology to produce steeper walls or trenches to reduce tapered structures which take up silicon real estate (chip area) and an optical wafer stepper to reduce the design rules from three to less than two microns. Rideout [296] and Chatterjee [299] have also reviewed these DRAM advances.

The 256K DRAM further reduced the design rule to the 1.5-2 μm range and introduced refractory metal silicides to reduce the interconnect wiring delay [44] and aluminum metal for double and triple polysilicon technologies. The M-bit DRAM era, initially a shrink of the original 2 μm 256K DRAM design, approached 1 μm design rules (see Table 2); more importantly, however, was the introduction of two three-dimensional (3-D) trench charge storage capacitors (see Figures 9 and 10). Sah has noted that the goal of these 3-D capacitor designs was to reduce the planar area of the storage capacitor while maintaining the storage capacitance at more than 32 fF to hold more than 10^6 electrons at a V_{DD} of 5V to limit soft errors [44]. In the stack capacitor design, multilayers of conductors (poly Si or Al) and insulators (silicon dioxide and silicon nitride) are stacked on top of the pass transistor. In the trench capacitor design, a trench is etched in the silicon and an MOS storage capacitor is fabricated in the trench, adjacent to the pass transistor which remains on the planar surface. In this

case, the trench depth is about 10 μm and the spatial area is about 6-9 μm^2 . Chatterjee and colleagues at Texas Instruments introduced a structure which placed the pass transistor inside the trench to further conserve silicon real estate [300,301].

The 4M DRAM era introduced the sub-micron design rule regime at 0.8 μm with 3-D storage capacitors. The types and features of storage cell designs have subsequently proliferated [44,302,303]. The decreasing design rules result in higher speed and reduced power-delay product as a result of lower capacitance and current [44]. The power-delay product is additionally reduced by reducing V_{DD} [44].

The DRAM became the test vehicle par excellence to advance the silicon IC process technology because of its repetitive memory structure. In more recent years, however, especially after the U.S. makers retreated from a significant position in the manufacture of DRAMS, their expertise in the fabrication of microprocessors has propelled the logic and microprocessor family as test vehicle drivers. Nevertheless, the DRAM continues to drive the extendibility of personal computers (PCs) vis-à-vis the memory content.

Integrated Circuit Scaling

Gordon Moore's remarkably prescient assessment of memory component growth in 1965, initially based on bipolar and then MOS memory density, observed that a semilog graph of the number of bits on a memory IC versus the date of initial availability was a straight line, representing almost a doubling per year [50-53]. Accordingly, a quadrupling was deduced every two years (consistent with the needs of the system houses) and subsequently modified to ≈ 3 years around the mid-later 1970s and currently taken as 3-4 years based on a 1995 assessment [53]. This analysis became enshrined as

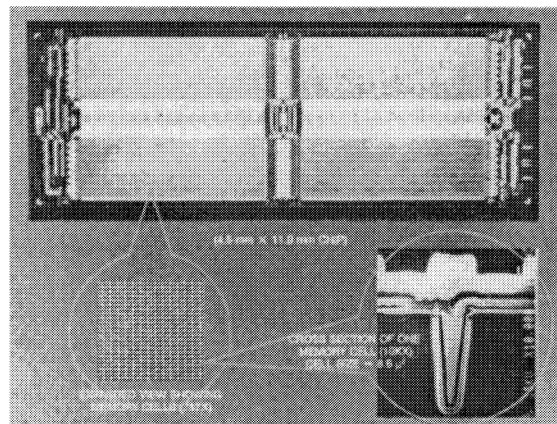


Figure 9. One Mbit CMOS DRAM chip, courtesy of Texas Instruments Incorporated.

Moore's law and became the productivity criterion by which the IC industry grew at $\approx 16\%$ compound annual growth rate (CAGR), facilitated by the availability of larger-diameter silicon single crystals to support the requisite larger chip sizes.

achieved. The cost effectiveness of international standards for emerging technologies such as SOI and 300 mm diameter wafers, in conjunction with the cost-effective production of ICs, such as computer-based design for manufacturability, will offer

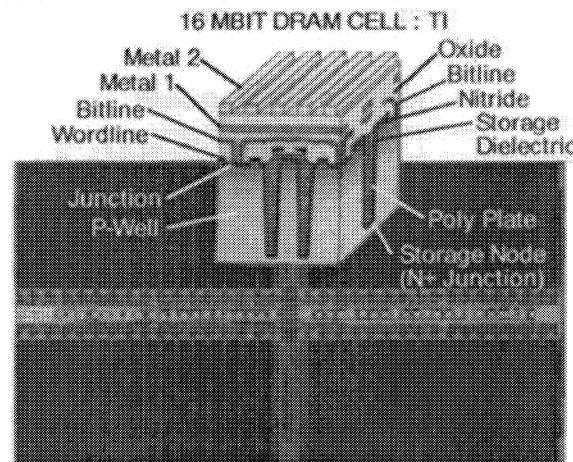


Figure 10. 16 Mbit DRAM cell, courtesy of Texas Instruments Incorporated.

The phenomenal growth of the IC industry, achieved by staying on the “productivity learning curve,” continues to be the gauge by which the industry is measured [55,304]. This is evidenced by the cost per bit or logic function historically declining at $\approx 16\%$ CAGR for the past several decades. This growth has been fueled by four factors; shrinking lithographic design rules, yield improvements, increased equipment utilization and larger wafer diameter. The largest opportunity growth factor to maintain the IC productivity engine and continue on the productivity curve as described by Moore's law appears to be increased equipment effectiveness; that is, the percentage of time the equipment is adding value to the wafer. The largest challenge to maintaining the productivity curve, however, may be the enormous financial infrastructure required, rather than technological limits to chip density. In that regard, business and manufacturing ideas will become increasingly important to ensure that the long-term productivity growth of the semiconductor industry maintains its growth near historical levels for the next ten years. More than just monitoring productivity, whether by staying on the productivity curve or increasing manufacturing effectiveness, however, is required. Rather, modeling productivity—the identification of new productivity measures—is required [56]. Global specifications, metrology and standards, in addition to CoO opportunities discussed earlier, are important mechanisms to ensure the marketplace reality of the ITRS roadmap trends, based on Moore's law, is

significant opportunities for an improved quality of life for the world's citizens. An even greater challenge to maintaining the productivity curve, however, may be the enormous financial infrastructure required, rather than technological limits to chip density [7,305]. This more recent development, regarding the escalating cost of building the IC fabrication facility, has been described, somewhat erroneously, as Moore's second law [306]. Indeed, a state-of-the-art IC fab producing 65 nm physical gate length MOSFET ICs (130 nm technology generation) is about \$2.5B (U.S.). The financial investment for implementation of the 300 mm and 450 mm wafer eras will certainly exacerbate this concern. Accordingly, ingenious engineering advancements to ensure the requisite number of chips per wafer (currently 200 mm in mainstream manufacturing) without introducing the next wafer diameter size, (i.e., 300 mm and, eventually, 450 mm) with the requisite increased chip performance, continues unabated. Nevertheless, the onset of the 300 mm era has begun for those IC manufacturers who anticipate a distinct cost advantage in going to the larger diameter wafer.

Device scaling has been the engine driving this revolution, based in large part on Robert Dennard's one-transistor memory cell introduced in 1968 [45]. The one-transistor/one-capacitor (1T1C) cell, in conjunction with the scaling methodology introduced by Dennard et al. in 1974 [46-49] (i.e., reduction in design rules without compromising the current-voltage characteristics) established the paradigm by

which enhanced scaling has progressed and facilitated the explosive growth and applications of the MOSFET IC. The original scaling methodology, based on constant electric field scaling principles, was generalized in 1984 to allow the voltage to be scaled less rapidly than the dimensions by increasing the electric field (with its own scaling factor) [46-49] (see Table 3). Major scaling contributions have

same, even if the field ϵ_f increases, and that the threshold voltage, V_t , is scaled down by the same factor as the applied voltage, V_{DD} . The active power for a given circuit scales as $\epsilon^2/\alpha_d\alpha_w$ while the power density scales as $\epsilon^2/\alpha_w/\alpha_d$, assuming that the clock frequency does indeed increase by α_d and that the same circuit designs are used.”

Table 3: Generalized Scaling Approach [49]. Reproduced by permission of The Electrochemical Society, Inc.

Physical Parameter	Generalized Scaling Factor
Channel length, L	$1/\alpha_d$
Gate insulator, T_{OX}	$1/\alpha_d$
Voltage, V	ϵ / α_d
Wiring width	$1/\alpha_w$
Channel width, W	$1/\alpha_w$
Circuit speed (goal)	α_d
Circuit power	$\epsilon^2 / \alpha_d \alpha_w$

occurred in the reductions of gate dielectric thickness, physical gate length and extension junction depth, as discussed by Dennard and colleagues via constant electric-field scaling and, subsequently, constant voltage scaling [47-49]. Dennard has recently summarized several aspects of the generalized scaling relationships [49]:

“The original constant-electric-field scaling principles which we introduced in the early 1970’s were generalized in the 1980’s to allow voltages to be scaled less rapidly than dimensions by increasing the electric field, which has its own scaling factor ϵ [47-49]. Another generalization can be made by allowing some basic device parameters and the interconnecting wire dimensions to be scaled down by different factors.

With these changes, our current view of scaling is shown in Table 3. Most device physical dimensions are divided by a factor of α_d and the voltage is scaled down by α_d but multiplied by the factor ϵ_f as discussed above. The wiring dimensions and the device width are divided by a factor α_w . A reasonable goal is to increase the circuit speed by a factor α_d , which assumes that the average carrier velocity remains about the

Evolving Directions

The gate dielectric thickness, physical gate length and extension junction depth parameters were empirically related in 1980 by Simon Sze and colleagues [307] to ensure the retention of long-channel behavior (i.e., no short-channel effects, such as V_t roll-off). For example, consider the scaling of the Kbit DRAM from the early 1970s (4K DRAM) to today’s leadership, high-performance MPU part appropriate for the 90 nm technology generation in 2003 [55]. The SiO_2 gate dielectric has decreased from the range of about 50-100 nm for the 4K DRAM to an anticipated value of about 1.2 nm oxide equivalent thickness (EOT) for the MPU part [55]. Likewise, the physical gate length has decreased from 7.5 μm for the 4K DRAM to a physical gate length of about 45 nm for the MPU part at the 90 nm technology generation [55]. Finally, the junction depth has decreased from several microns for the 4K DRAM to about 20 nm for the extension junction depth for the MPU part at the 90 nm technology generation [55]. In a related fashion, the critical figure of merit for transistor speed, CV/I , has become less than one psec for an NMOSFET and typically approaching one psec (or slightly less) for a PMOSFET, as the MOS physical gate length has decreased from 30 nm to 10 nm, the latter dimension being appropriate for the 64G DRAM and 9 G high-

performance logic era in 2016 [55]. It is anticipated that the “silicon age” of IC microelectronics has a sufficiently robust, but challenging future.

Scaling of the gate dielectric SiO₂ to the sub-2 nm regime, however, has exacerbated the occurrence of direct tunneling [308,309] as described by Yuan Taur and colleagues. An extensive global effort is in progress by numerous personnel [310-315] to identify an alternative, high-dielectric constant material to circumvent the gate dielectric direct tunneling leakage current when the silicon oxynitride gate dielectric physical thickness is less than about 1.2 nm for high performance microprocessors, including the relevant diagnostic techniques [8]. Additionally, the importance of gate electrodes (eventually requiring dual metal gates with differing work functions for CMOS optimization or a single, tunable work function metal) and the issues of incorporating the gate stack into an integrated, conventional planar, initially poly electrode, IC process flow has been noted [315]. Al Tasch has clarified the role of the quantum confinement effect in silicon in increasing the effective dielectric thickness of a MOSFET in inversion [316], which cannot be avoided as compared to the poly-depletion effect in the polysilicon gate electrode, which can be negated by utilizing metal gate electrodes. In that regard, the dual metal system with differing work functions is under consideration as the gate electrodes for optimal CMOS performance [55].

Concurrently, a host of studies are in progress to identify an ultrashallow junction fabrication methodology consonant with the sub-90 nm technology generations [55,317]. These studies may be grouped under the classification as classical CMOS structures. On the other hand, a plethora of non-classical CMOS devices are under consideration wherein a unique combination of materials and/or device structural configurations may differ from the conventional or classical planar CMOS structure [55,57]. Of particular importance is the assessment of alternate channels for enhancement of the n- and p-channel mobility, ranging from strained silicon on unstrained Si-Ge on SOI, silicon-germanium on silicon and a host of alternative vertical transistor structural configurations [318,319] as well as the semi-ballistic transistor [320].

Accordingly, silicon MOSFET's may be expected to scale in an essentially predictable manner from the present state-of-the-art 90 nm technology generation (MPU physical gate length of 45 nm) to the 22 nm technology generation (MPU physical gate length of 9 nm) [55]. Concurrently, the IC industry has continually seen that the ingenuity of device and process engineers to develop unique device geometries, from the early DRAM era [44] and, more recently, non-classical CMOS devices including

vertical transistor configurations or double-gate structures utilizing SOI as appropriate, novel process technologies and models to guide further development may be more influential to IC growth and device performance than might be inferred from the extrapolation of today's art [57,321,322] and may offer significant unforeseen opportunities. The ubiquitous applicability of Si technology in the information revolution, touching numerous aspects of the lives of the worlds' citizens, however, may not necessarily require the state-of-the-art technologies in all applications [7,8]. It is unlikely, moreover, that the present worldwide silicon infrastructure will be regenerated to support a silicon successor [323]. Accordingly, silicon technology is expected to continue as the most powerful driver of the information age for at least the next 100 years, albeit in conjunction with complementary, alternative device structures.

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