1384 LOGIC CLOCK 60Hz to 50Hz CONVERSION

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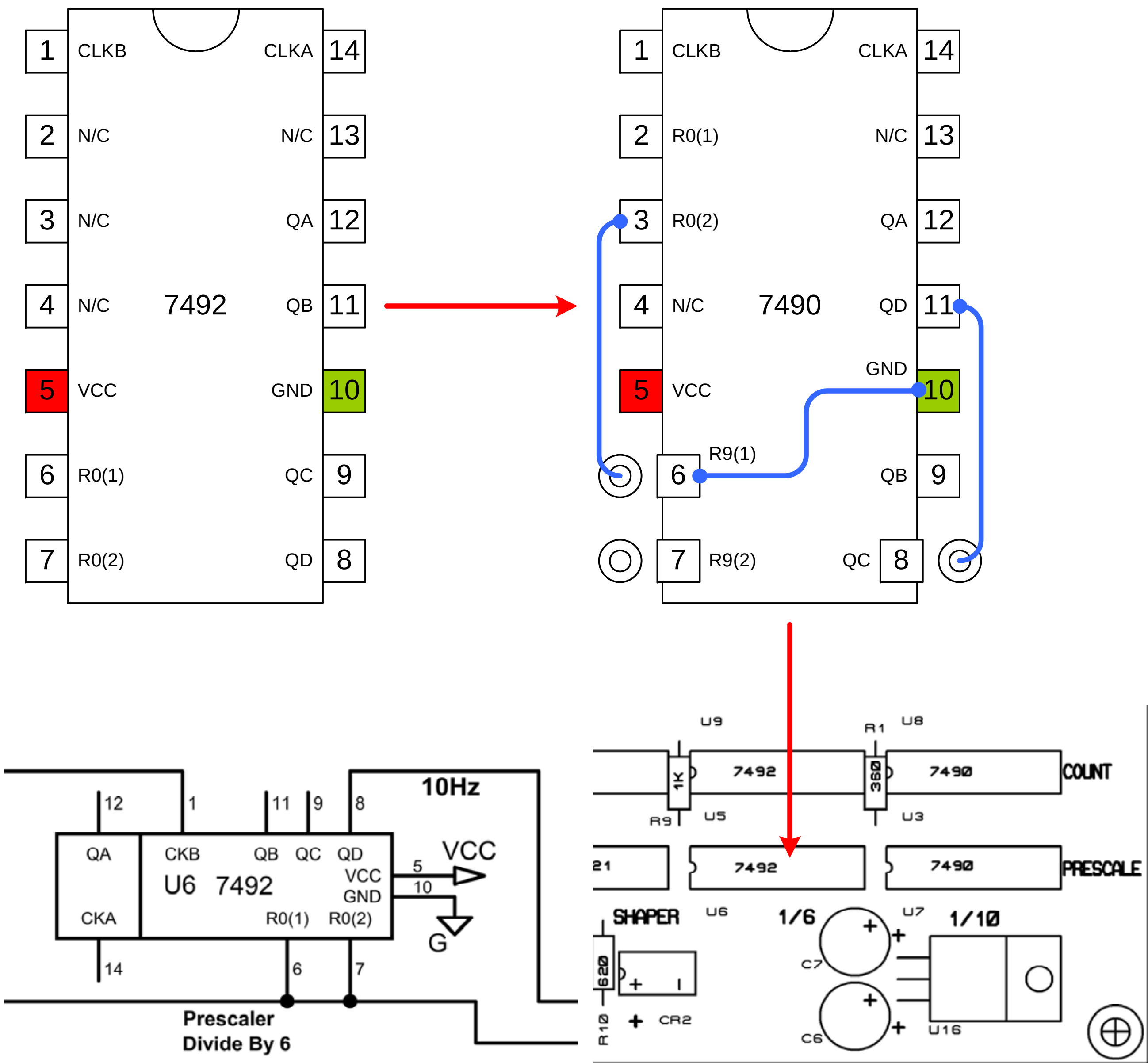

The clock was designed for 60 Hz operation and uses the Div-by-6 stage of $U6_{7492}$ and $U7_{7490}$ to prescale the line frequency to 1 Hz: $U6_6 \times U7_{10} = 60$.

To convert the clock to 50 Hz, you need to change the line prescale from 60 to 50 by changing U6 to a 7490 to use its Div-by-5 stage: $U6_5 \times U7_{10} = 50$.

1. Remove (Or do not install) the 7492 in position U6.

2. Prepare a 7490 counter by bending leads 6, 7 and 8 up over the top.

3. Install the prepared 7490 into position U6, being sure leave the empty PWB holes accessible.

4. Jumper pin 3 to the open hole for pin 6 to connect the count hold signal.

5. Jumper pin 11 to the open hole for pin 8 to connect the QD output to the U7 clock input.

6. Jumper the bent up pin 6 to the ground pin 10 to disable the Reset-9 function.