Section 1: SmartNixie Overview

The TES SmartNixie is a family of self contained I²C addressable nixie modules. With the on board 4 position DIP switch the I²C slaves may be set for addresses from 0x10 to 0x1E (8 slaves) or the lower address inputs A_0 and A_1 can be configured to be read as analog inputs. In the analog input mode, slave addresses can range from 0x10 to 0xEE (112 slaves) where addresses 0x10 to 0x1E are the same as for the digital input mode. So long as the resistor dividers that set the analog address operate from the same Vdd as the module, only the resistor tolerance is a factor in the accuracy of the internal address computation.

The first eight analog device addresses put the SmartNixie module into one of eight special operating modes, i.e. Mode 5 is "Ripple counter" where modules can be connected as shown in Figure 8 to build counter chains of any length. See Table 3 for the complete special mode list.

When the A_3/A_2 address inputs are set to 1/1, the SmartNixie module operates as a master I²C device, controlling five other slave modules to create one of two simple six digit clock designs. Figure 12 illustrates the simplest version which uses an external 50/60Hz line reference for time keeping showing time in a HH:MM:SS format. Figure 13 illustrates a slightly more complex configuration which uses a stand alone Real Time Clock IC and on board back up battery for greater than 2 years of unpowered timekeeping as well as a perpetual calendar function.

The SmartNixie modules operate from a Vdd from 3.0 to 5.5VDC and communicate on the I²C bus at 100Kbps. Typical supply current into Vdd is < 2.5mA at 5.5VDC. The nixie anode supply is 170V typical, cathode drivers are rated 240V and 100mA sink current with only 100nA of off current at 240VDC.

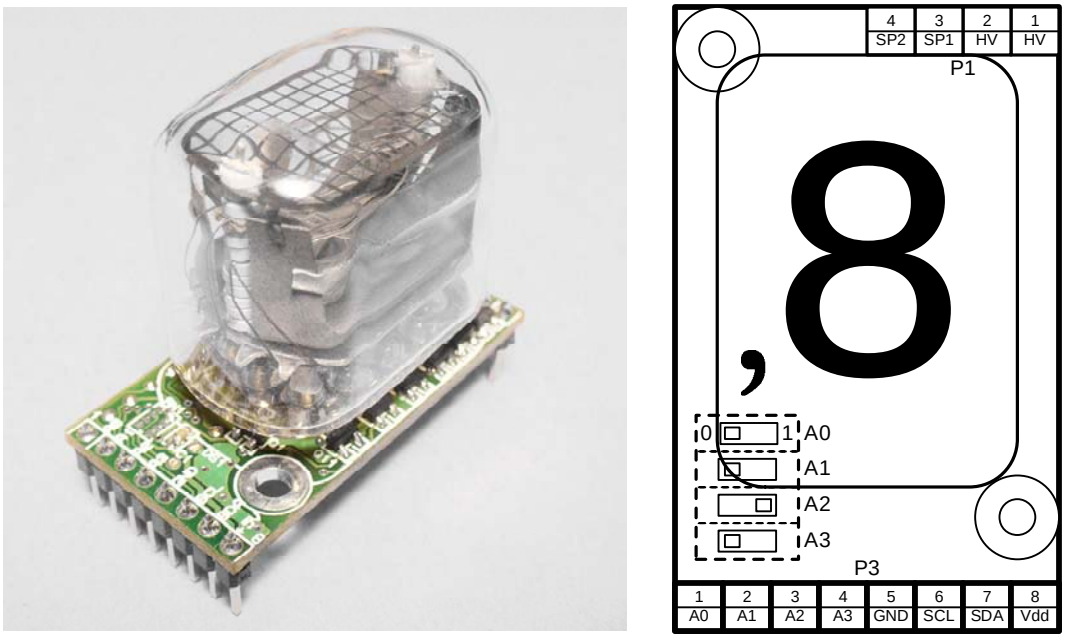


Figure 1: SmartNixie (-IN12 module shown)

Table 1a: Pin Descriptions -IN12

Pin		Name	Description
P1	1	HV	+170V nixie anode voltage
	2	HV	Connected to pin 2
	3	Spare1	Comma cathode for IN12B
	4	Spare2	Aux cathode driver
P3	1	A0	Address 0 of module[1]
	2	A1	Address 1 of module[1]
	3	A2	Address 2 of module[2]
	4	A3	Address 3 of module[3]
	5	GND	Power input, 0V
	6	SCL	I^2C serial clock (I^2C Mode)
	7	SDA	I^2C serial data (I^2C Mode)
	8	Vdd	Power input, 3.0V-5.50V

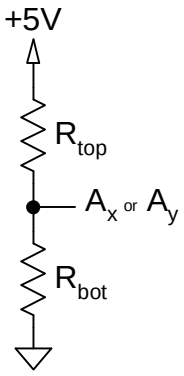
Notes:

1. When A3/A2 are 0/0, 0/1 or 1/1 these pins are configured as digital inputs pulled up to Vdd with a 50-450uA current. When A3/A2 are 1/0 these pins are configured as analog inputs with no pull ups.
2. A2 is always pulled up to Vdd with 100K.
3. A3 is always pulled up to Vdd with a 50-450uA current.

Section 2: SmartNixie Addressing

Table 2: Module Addressing

DIP Switch					
A_3	A_2	A_1	A_0	Base Addr	Description
0	0	0	0	**0x10**	Simple slave addressing, DIP switch is read as digital input with pull ups active.
0	0	0	1	**0x12**	
0	0	1	0	**0x14**	
0	0	1	1	**0x16**	
0	1	0	0	**0x18**	
0	1	0	1	**0x1A**	
0	1	1	0	**0x1C**	
0	1	1	1	**0x1E**	
1	0	0	A_y		See Table 3 for special modes
1	0	A_x	A_y	**0x10-0xEE**	Extended slave addressing...



Ex Values
6.19K-1%
10.0K-1%
13.3K-1%
15.0K-1%
38.3K-1%
130K-1%

Ax and Ay are configured as analog inputs without pull-ups in this mode, where the unit base address can be computed from...

$$(((Bin_{Ax} \times 11) + Bin_{Ay}) \times 2) - 2$$

...yielding 112 unique slave base addresses ranging from **0x10** to **0xEE**.

The Voltage Bins are defined as follows with example resistor divider values shown such that only 6 different 1% values are required:

Bin	Voltage	Rtop	Rbot	Rtot	I-uA
0	0.227	130K	6.19K	136K	37
1	0.682	38.3K	6.19K	44.5K	112
2	1.136	130K	38.3K	168K	30
3	1.591	13.3K	6.19K	19.5K	256
4	2.045	15.0K	10.0K	25.0K	200
5	2.500	38.3K	38.3K	76.6K	65
6	2.955	10.0K	15.0K	25.0K	200
7	3.409	6.19K	13.3K	19.5K	256
8	3.864	38.3K	130K	168K	30
9	4.318	6.19K	38.3K	44.5K	112
10	4.773	6.19K	130K	136K	37

The A/D conversion is 10 bits so that the above values give better than +/-30 counts of margin beyond the resistor tolerance limits.

1	1	m	m		Clock modes, see Table 3

Notes:
1. Voltage bins shown are based on 5V into Vdd but are actually ratiometric such that the same divider resistors will yield the same address/mode for any Vdd within the allowed operating range.

Section 2: SmartNixie Addressing

Table 3: Module Addressing, Special Modes

DIP Switch				A_y Value			
A_3	A_2	A_1	A_0	Bin	Volts	Mode	Special Mode Description: I^2C is disabled
1	0	0	A_y	0	0.227	**0**	Burn-in counter free running at 10Hz (Figure 3)
				1	0.682	**1**	Reserved for future use
				2	1.136	**2**	Reserved for future use
				3	1.591	**3**	Reserved for future use
				4	2.045	**4**	Reserved for future use
				5	2.500	**5**	Ripple counter: A2=/Reset, SDA=CKin, SCL=CKout (Figure 8)
				6	2.955	**6**	Reserved for future use
				7	3.409	**7**	Reserved for future use
				8	3.864	**8**	Version/Serial# stream on SCL, Async 19.2Kbps (Figure 11)
				9	4.318	**0x10**	*Standard mode slave address = 0x10*
				10	4.773	**0x12**	*Standard mode slave address = 0x12*
1	1	0	x	---	---	**9**	6 digit clock master with 60Hz reference into A_0 (Figure 12)[3]
1	1	1	x	---	---	**10**	6 digit clock/calendar master using PCF8563 RTC (Figure 13)

Notes:

1. Voltage bins shown are based on 5V into Vdd but are actually ratiometric such that the same divider resistors will yield the same address/mode for any Vdd within the allowed operating range.
2. Reserved mode addresses operate as the Burn-in counter mode when selected.
3. The default line frequency is 60Hz but 50, 60 and 100Hz line clock dividers are selectable via the clock setting controls.

Section 3: SmartNixie Applications

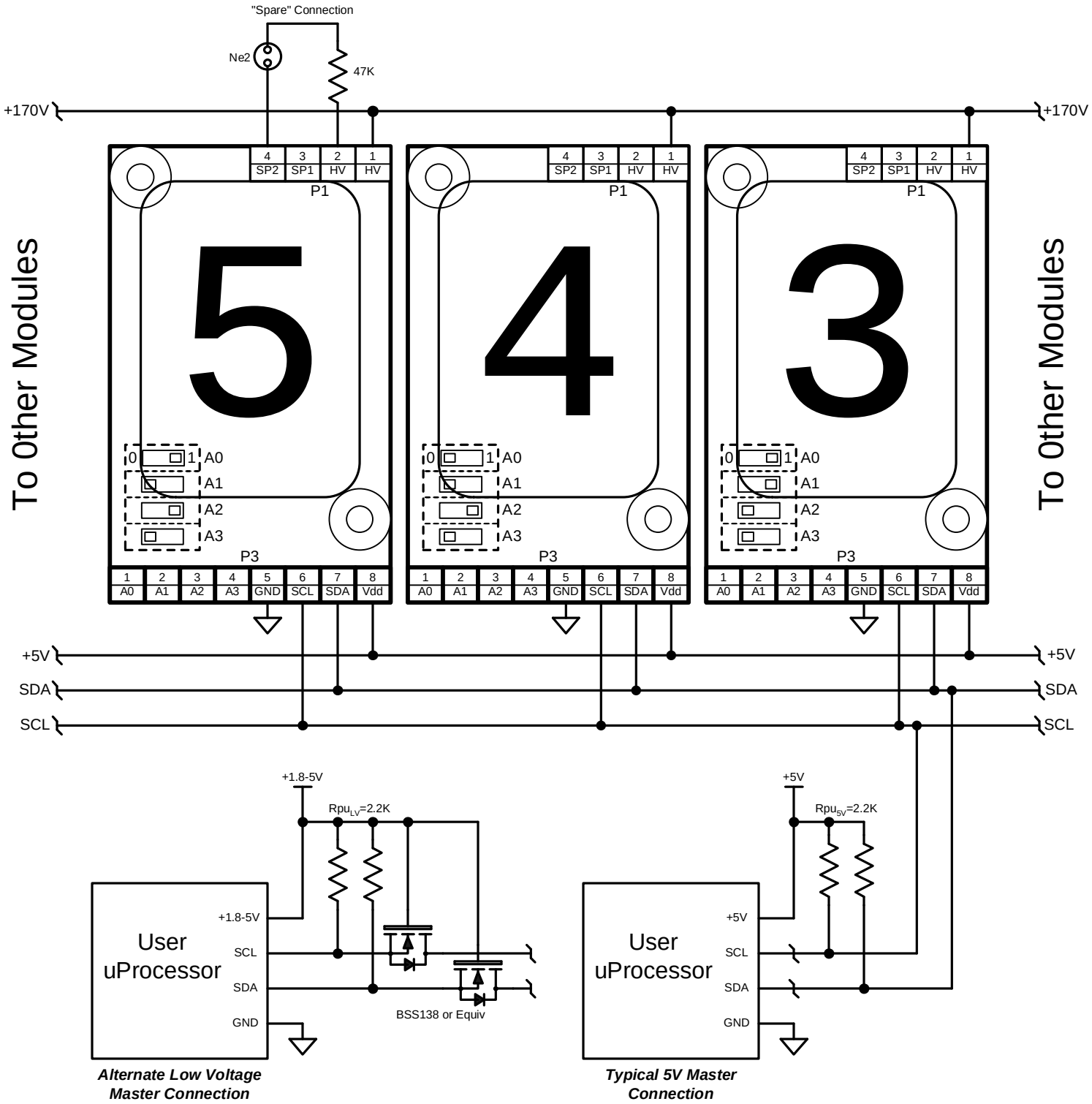
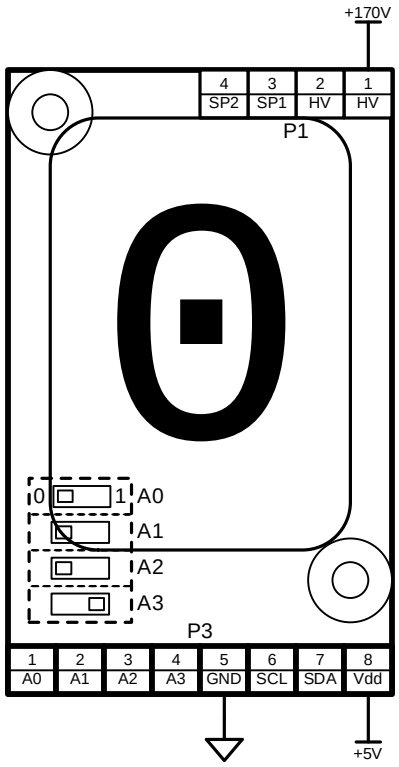


Figure 2: Typical Slave Bus Connection (Addr=0x10 to 0xEE)

Section 3: SmartNixie Applications



Unit will count 0-9 at
about a 10Hz rate

Figure 3: Stand Alone Burn-in Counter (Mode=0)

Section 3: SmartNixie Applications

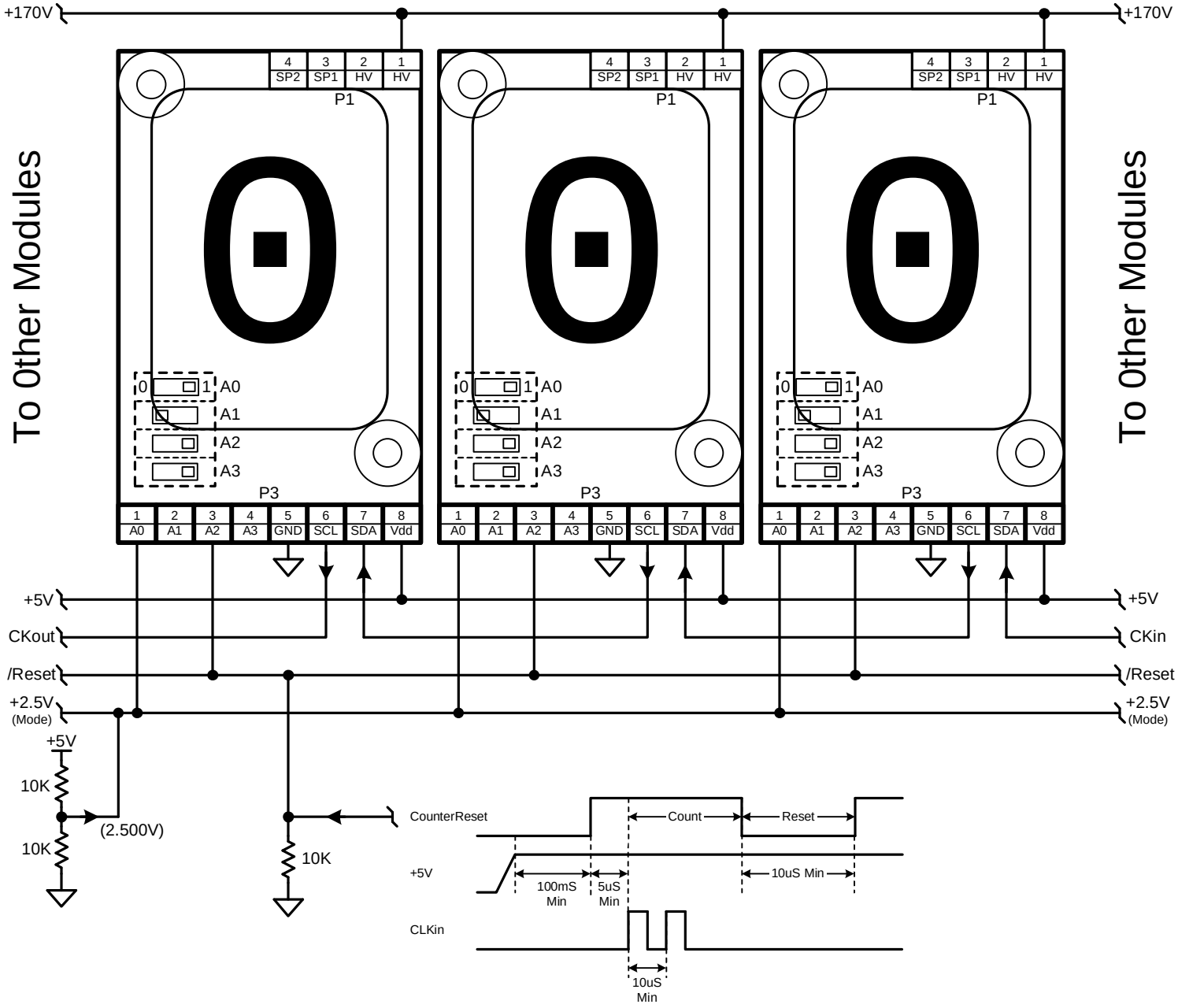


Figure 8: Ripple Counter Mode Connection, No Dimming (Mode=5)

Section 3: SmartNixie Applications

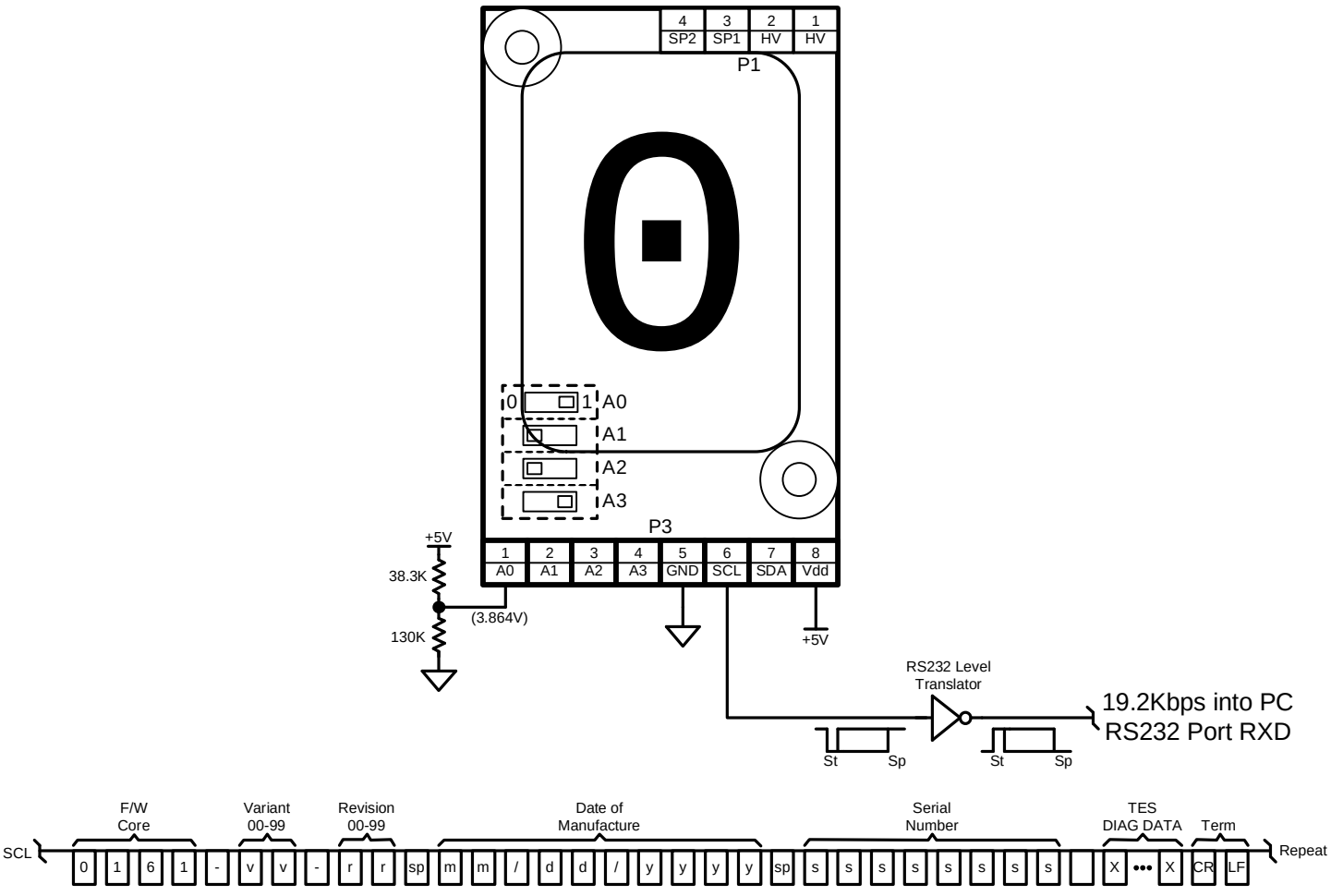


Figure 11: Serial Number / Version Data Stream (Mode=8)

Section 3: SmartNixie Applications

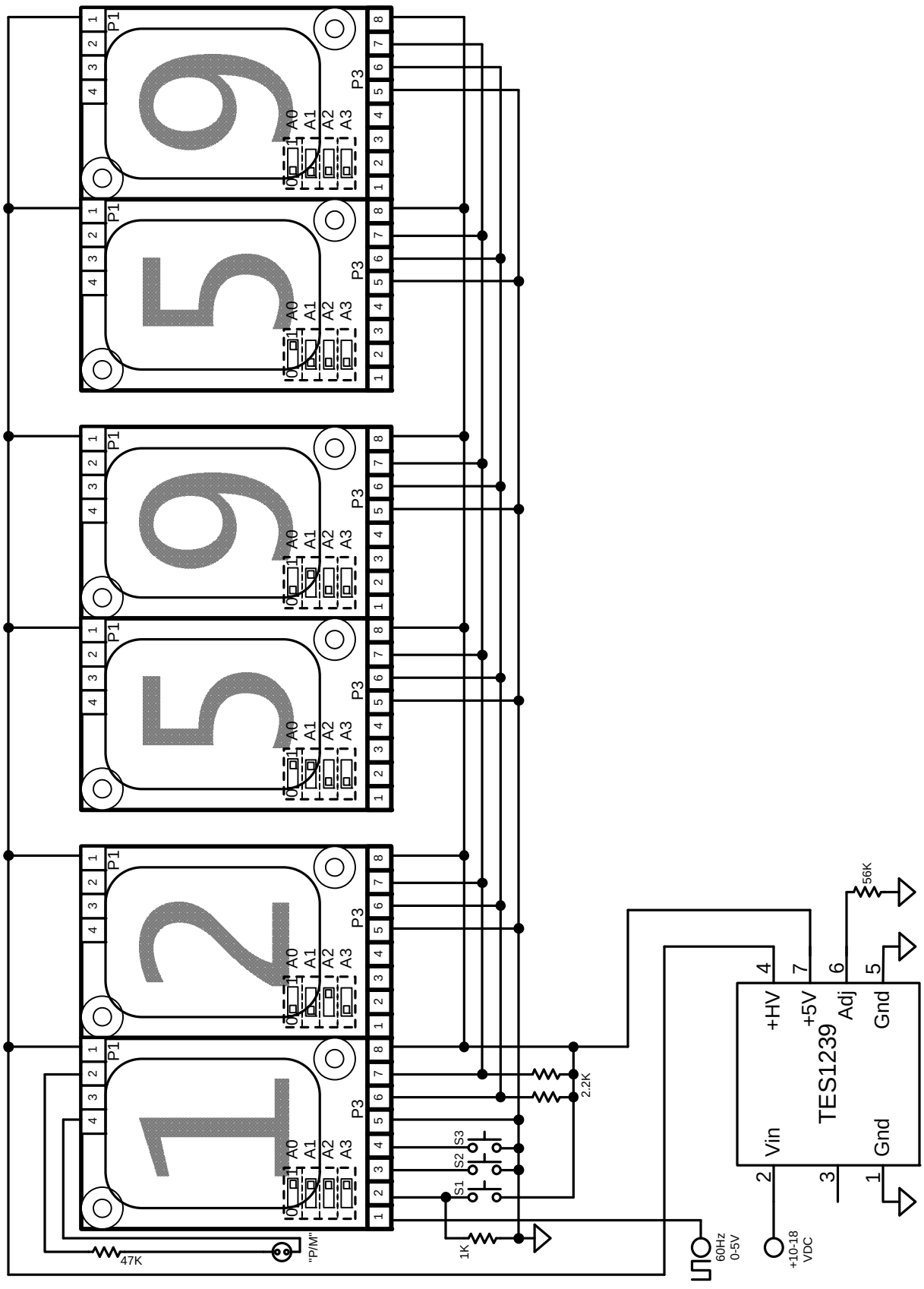


Figure 12: 60Hz Reference Clock (Mode=9)

Section 3: SmartNixie Applications

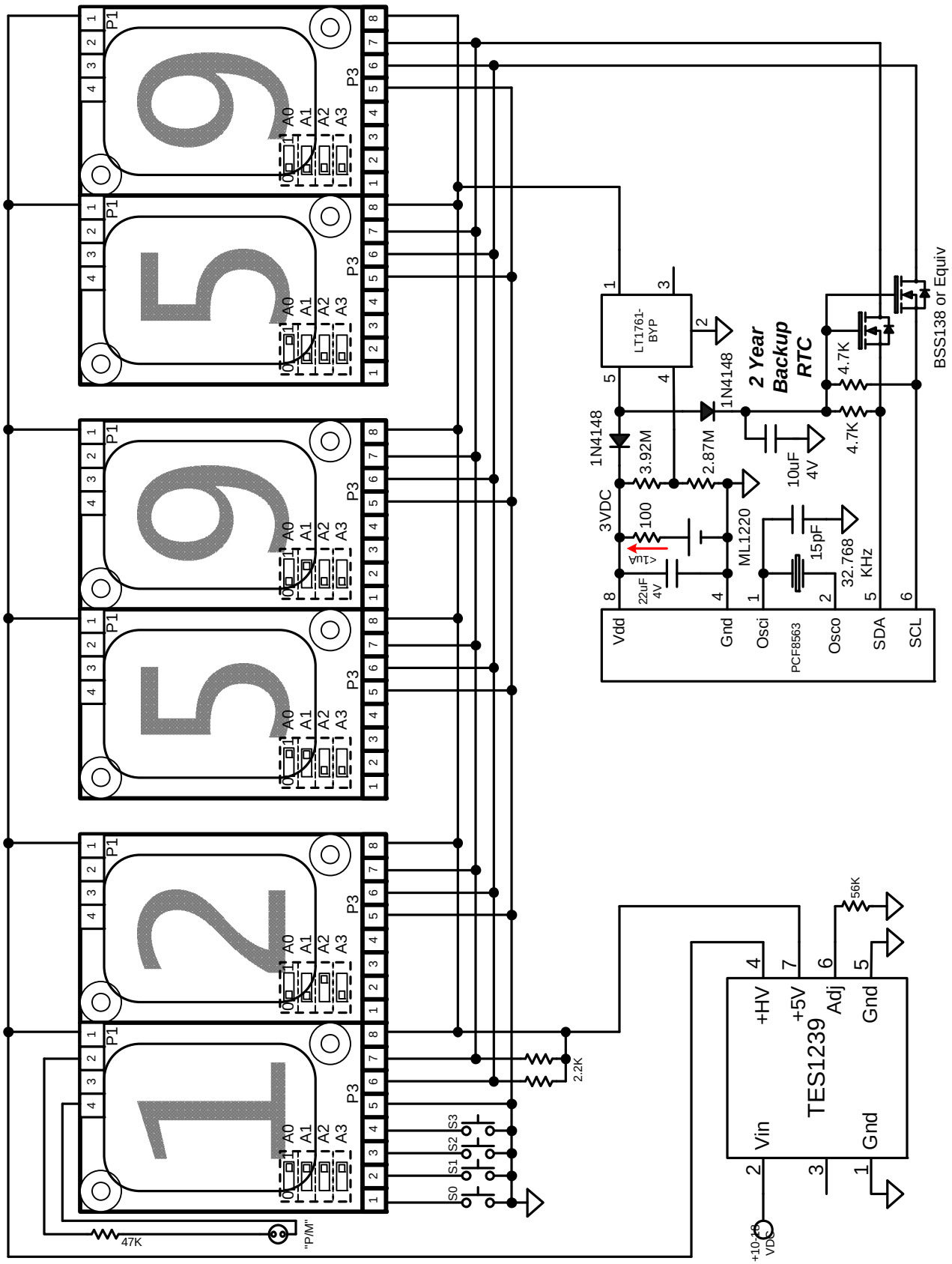


Figure 13: Stand Alone Clock/Calendar (Mode=10)

Section 3: SmartNixie Applications

Table 4: Clock setting (Modes 9 and 10)

Button Press					Display						
S3	S2	S1	S0	Function Description	Mode	Mode	---	---	10's	1's	Function
			X	Show date in format MM:DD:YY (Only available in RTC clock Mode 10)							
X				Hold for >2 seconds to enter setting mode (Was 5 seconds for 1.02 FW)							
X				Hold for >2 seconds to exit setting mode, executes upon release							
X				Press >150mS and <2 seconds to advance to next setting selection							
					0	0	---	---	H	H	Hours
					0	1	---	---	M	M	Minutes
					0	2	---	---	S	S	Seconds
					0	3	---	---	Mo	Mo	Months
					0	4	---	---	D	D	Days
					0	5	---	---	Y	Y	Years
					0	6	---	---	C	C	12/24 hour clock select (12/24)[1/6]
					0	7	---	---	L	L	Mode 9 Clock Master line frequency select[1/6]
									0	0	No prescale, free-run clock
									0	1	Divide-by-1
									1	0	Divide-by-10
									5	0	Divide-by-50
									6	0	Divide-by-60
									5	2	Divide-by-100 (50 x 2)
									6	2	Divide-by-120 (60 x 2)
									9	9	Divide-by-255
					0	8	---	---	8	8	Dimmer setting, 10-100%[2/6]
	X			Advance 10's digit[3]							
		X		Advance 1's digit[3]							

Notes:

1. S1 and S2 perform the same function of stepping through the available selections.
2. Displays "88" at the current dimming level while the mode display remains at 100% brightness. In this mode, S2 and S1 increase and decrease the brightness level respectively. Upon exiting the setting mode the entire display is set to the selected brightness level.
3. Holding the advance buttons down auto increments at 150mS per step. Values are adjusted for setting limits, i.e. seconds may only be set from 00 to 59 and months may only be set from 01 to 12 however no test is done, for example, to ensure that you do not enter 31 days for November.
4. To align the clock time with an external reference, adjust ahead to an upcoming time, then hold S3 down for more than 2 seconds and release at the matching reference time.
5. Even though the date can be set in the Mode 9 configuration and the line frequency can be set in the Mode 10 configuration, these settings are ignored if not applicable to the clock mode as configured.
6. 12/24 hour mode, line frequency select and the current dimmer setting are stored in EEPROM and reloaded on power cycle.
7. For the RTC clock (Mode 10), exiting setting when the display shows "00 xx HH" will save only the configuration data such as dimming, time will not be updated. For the line clock (Mode 9), time is updated regardless of the current setting menu since time is not counted when in the setting mode.

Section 4: SmartNixie Communication

An I²C master communicates with groups of TES1328 modules configured as slaves via a sixteen element register stack using standard I²C commands at a maximum data rate of 100kbps. See Table 5 for a complete list of the slave stack register functions.

For register writes a Start command is issued followed by the slave address where the R/W bit is cleared to zero. The next byte written is the pointer to the desired element in the register stack from 0x00 to 0x0D where this pointer is automatically trimmed to the four LSBs. The next bytes written are the register data and after the last register data byte has been sent, a Stop command is issued which completes the transaction. Each write by the master is followed by a low ACK bit generated by the slave indicating an acknowledgement of the transaction, where a high NAK bit generally indicates no slave at the specified address is present.

After each write the internal register pointer is incremented allowing from one to fourteen consecutive registers to be written in the same transaction. Writes beyond the last writeable register position (0x0D) are ignored. Two byte registers are executed after the second (Low) byte has been received.

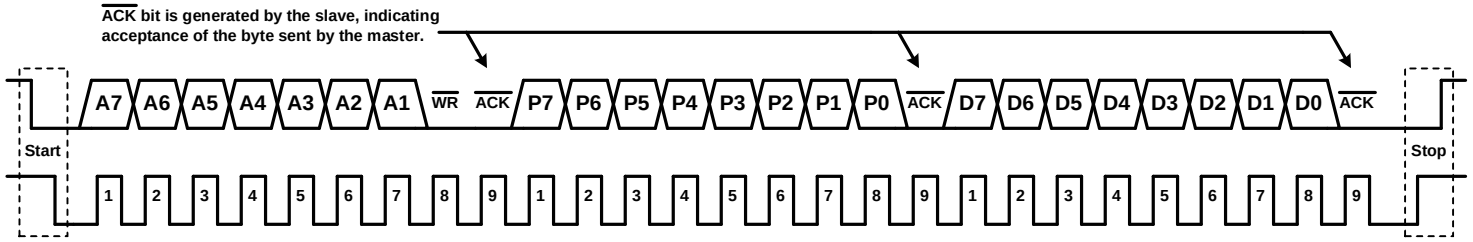


Figure 15: Typical Write Sequence

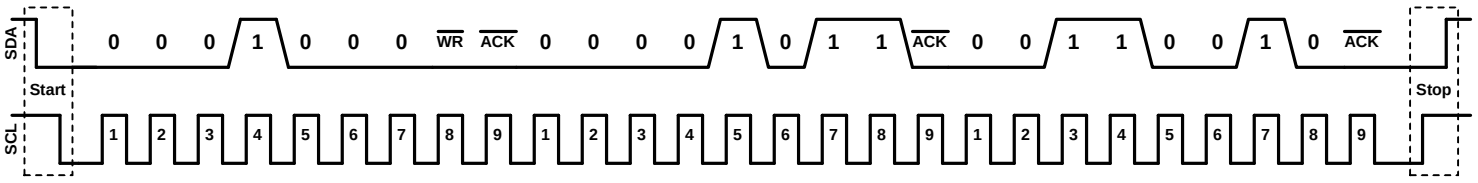


Figure 16a: Write to slave 0x10, Register 0x0B with Data 0x32 (50% dimmer)

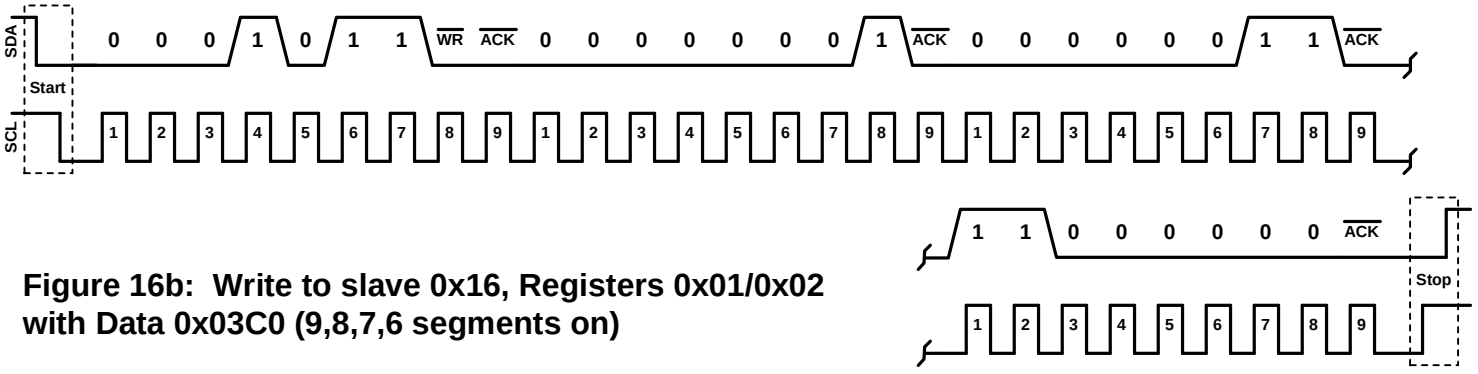


Figure 16b: Write to slave 0x16, Registers 0x01/0x02 with Data 0x03C0 (9,8,7,6 segments on)

Section 4: SmartNixie Communication

For register reads a Start command is issued followed by the slave address where the R/W bit is set to one. The first byte read is always register 0x00 and each additional read returns the next byte in the register stack from 0x01 to 0x0F where the internal pointer is automatically trimmed to the four LSBs so that the sixteenth byte read is register 0x00 and so on. After the last register has been read by the master, a Stop command is issued which completes the transaction. Each read by the master is followed by a low ACK bit generated by the master except for the last read which must be followed by a high NAK bit from the master signaling to the slave that no further bytes will be read.

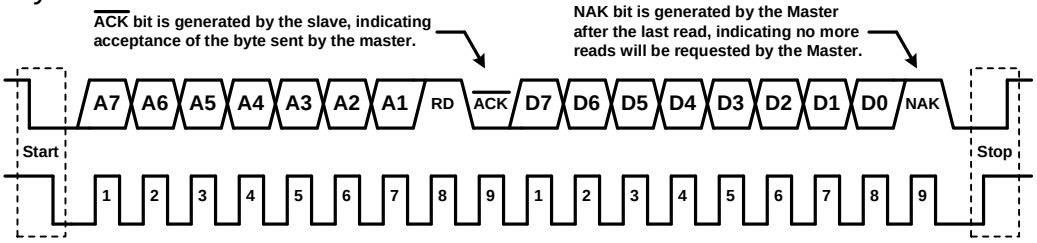


Figure 17: Typical One Byte Read Sequence

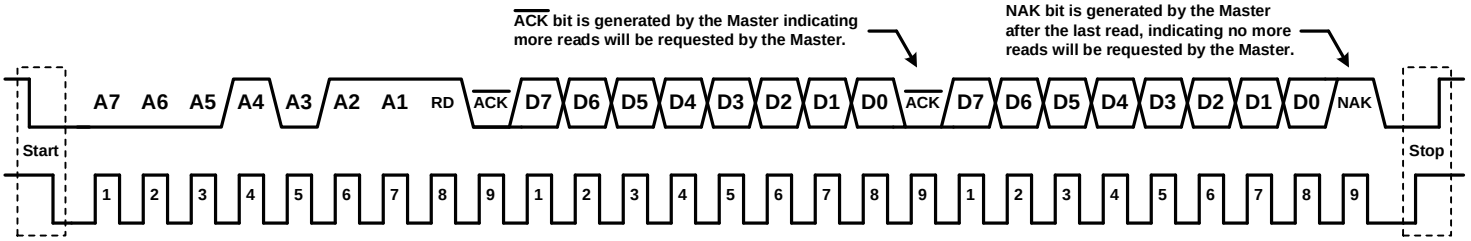


Figure 18a: Multi Byte Read Sequence from Slave 0x16

```
//PICC code for Figure 16a
I2C_START();
I2C_WRITE(0x10);        //slave address, R/W set low
I2C_WRITE(0x0B);        //register address=dimmer
I2C_WRITE(0x32);        //dimmer=50%
I2C_STOP();

//PICC code for Figure 16b
I2C_START();
I2C_WRITE(0x16);        //slave address, R/W set low
I2C_WRITE(0x01);        //register address=bitmap
I2C_WRITE(0x03);        //high byte, "9","8" on
I2C_WRITE(0xC0);        //low byte, "7","6" on
I2C_STOP();

//PICC code for Figure 18a
//Reads from slave always begin with register 0x00
I2C_START();
I2C_WRITE(0x17);        //slave address, R/W set high
data1=I2C_READ(0);      //reads register 0x00
data2=I2C_READ(1);      //reads register 0x01 (and so on)
I2C_STOP();             //  last read is always (1)=NAK
```

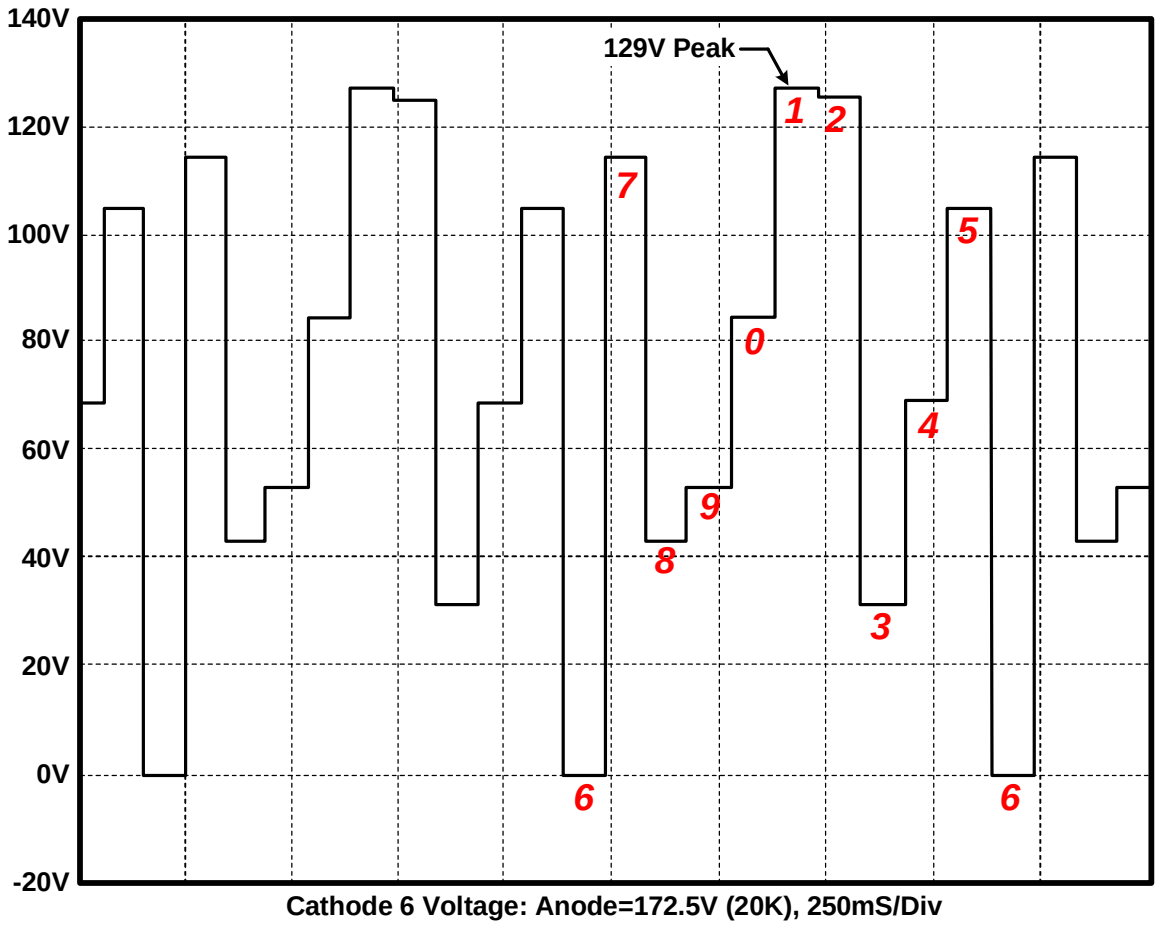
Figure 19: Example coding

Section 4: SmartNixie Communication

Table 5: Slave Mode Control Registers

Register	Name	Description
0x00	Character	0x00 to 0x0B select digits "0" to "9", "LHCM" and "Spare" respectively. (IN12A modules do not have LHCM segment).
0x01 0x02	BitmapHigh BitmapLow	Any combination of segments can be enabled, executed when the low register of the pair is written. Bits marked "x" are don't care (This is essentially the "Numitron" mode). BitmapHigh BitmapLow **7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 Character** x x x x 0 0 0 0 0 0 0 0 0 1 "0" x x x x 0 0 0 0 0 0 0 0 1 0 "1" x x x x 0 0 0 0 0 0 0 1 0 0 "2" x x x x 0 0 0 0 0 0 1 0 0 0 "3" x x x x 0 0 0 0 0 1 0 0 0 0 "4" x x x x 0 0 0 0 0 0 1 0 0 0 0 "5" x x x x 0 0 0 0 0 1 0 0 0 0 0 "6" x x x x 0 0 0 0 1 0 0 0 0 0 0 "7" x x x x 0 0 0 1 0 0 0 0 0 0 0 "8" x x x x 0 0 1 0 0 0 0 0 0 0 0 "9" x x x x 0 1 0 0 0 0 0 0 0 0 0 "LHCM" x x x x 1 0 0 0 0 0 0 0 0 0 0 "Spare" x x x x 0 0 0 0 0 0 0 0 0 0 0 (All off) x x x x 1 1 1 1 1 1 1 1 1 1 (All on)
0x03	StaticDimmer	Writes value to EEPROM dimmer register
0x04	StaticLineFreq	Writes value to EEPROM line frequency prescaler register
0x05	StaticClockMode	Writes value to EEPROM n12/24 hour select register
0x06-0x07	Reserved	Reserved for future use
0x08-0x0A	EEPROM	Factory EEPROM Control Register
0x0B	Dimmer	Display duty cycle from 0 to 100%: On time is (n x 100uS) + 100uS for a minimum illumination of 1% and a PWM frequency of 10Khz. 50% will be equal to a 10.1mS period of 50% duty cycle (~100Hz).
0x0C	Delay	Delay in 10mS units from 10mS to 2.55S used for the free running burn-in counter mode (Count increment timer) as well as the character flash mode (On/Off timer).
0x0D	Command	Command 0x00 Start burn-in counter 0x01 Stop burn-in counter 0x02 Start character flashing 0x03 Stop character flashing 0x96 Reset slave CPU
0x0E	FirmwareCore	Read Only: 161
0x0F	FirmwareRevision	Read Only: VRR Variant (0/1/2) and Revision (00-99)

Section 5: SmartNixie Electrical



Cathode 6 Voltage: Anode=172.5V (20K), 250mS/Div

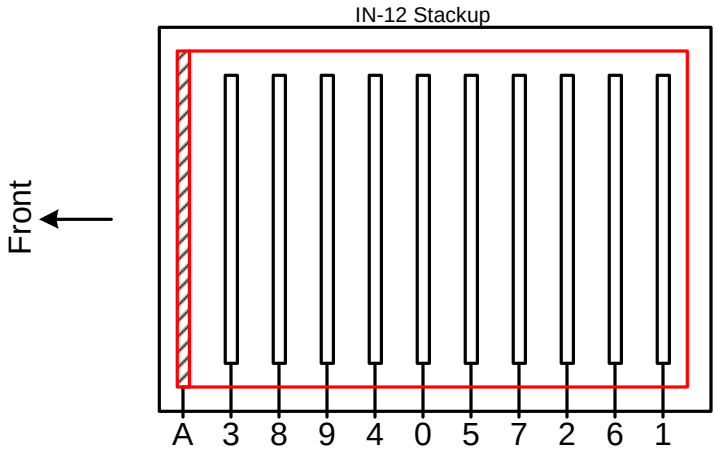


Figure 20: Burn-in Counting Mode Inter-Digit Coupling (-IN12 module signals shown)

Section 5: SmartNixie Electrical

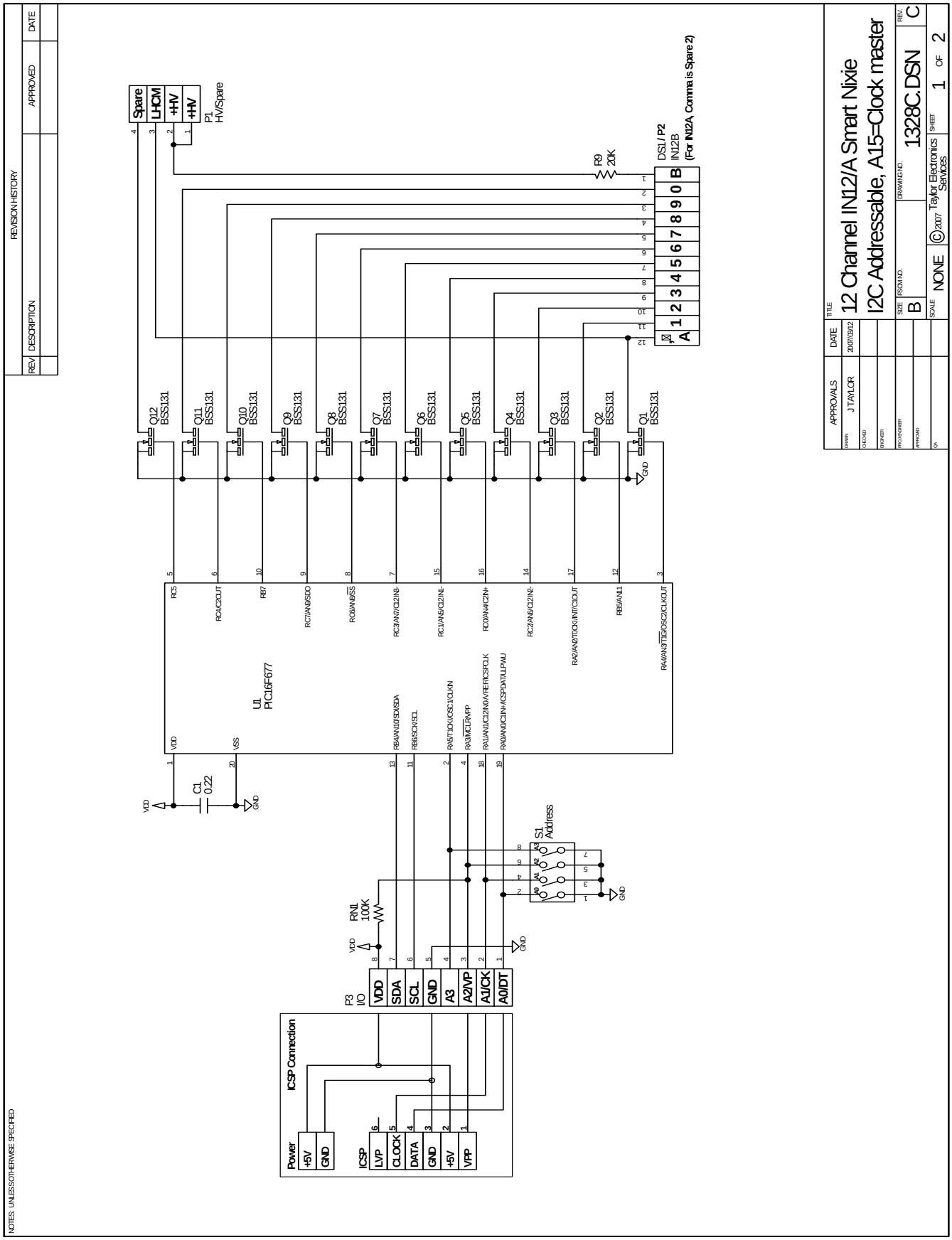


Figure 21: Schematic, SmartNixie-IN12

Section 6: SmartNixie Mechanical

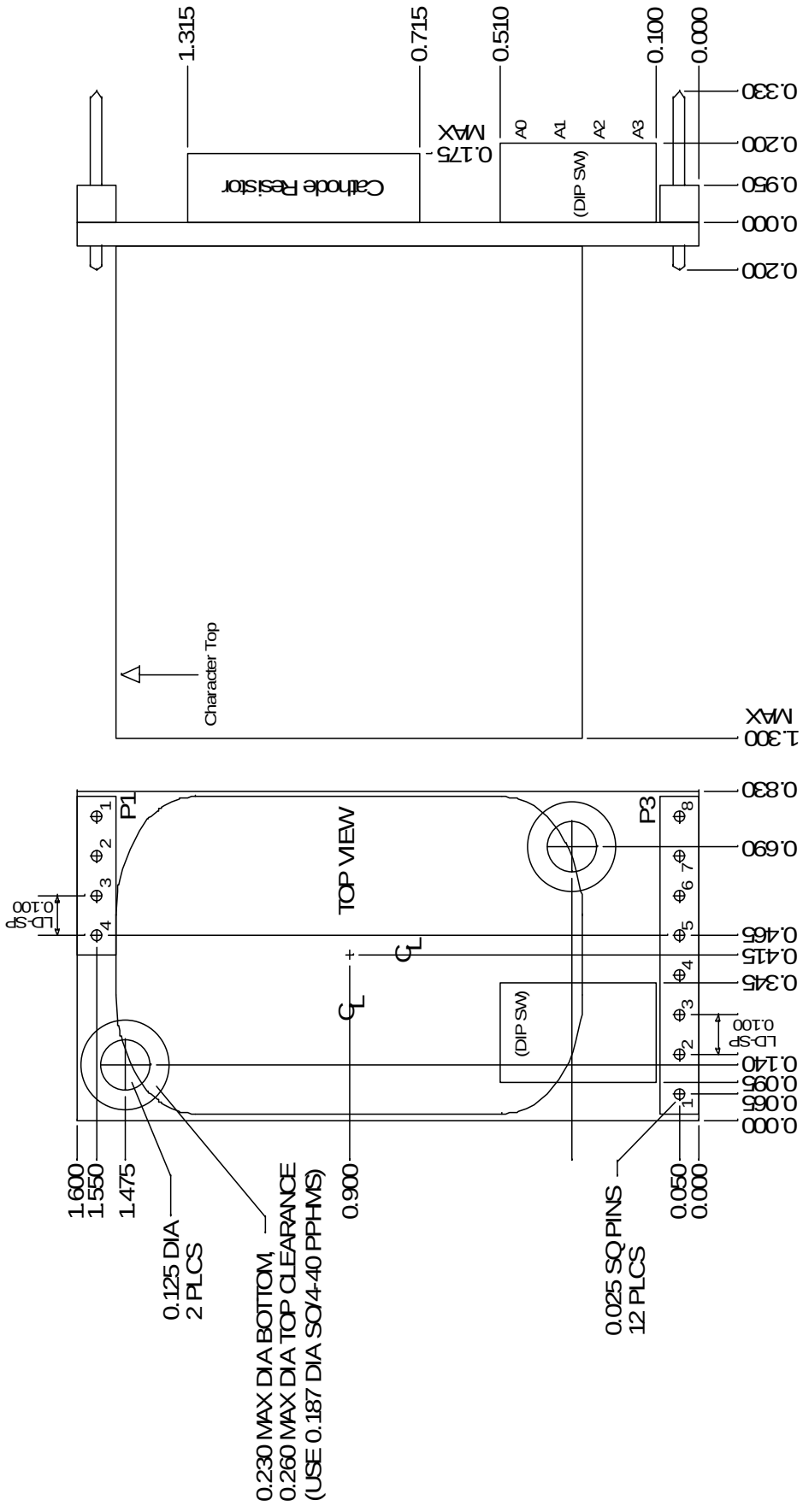


Figure 22: Package Outline, SmartNixie-IN12