

Section 1: SmartNixie Overview

The TES SmartNixie is a family of self contained I²C addressable nixie modules. With the on board 4 position DIP switch the I²C slaves may be set for addresses from 0x10 to 0x1E (8 slaves) or the lower address inputs A₀ and A₁ can be configured to be read as analog inputs. In the analog input mode, slave addresses can range from 0x10 to 0xEE (112 slaves) where addresses 0x10 to 0x1E are the same as for the digital input mode. So long as the resistor dividers that set the analog address operate from the same V_{dd} as the module, only the resistor tolerance is a factor in the accuracy of the internal address computation.

The first eight analog device addresses put the SmartNixie module into one of eight special operating modes, i.e. Mode 5 is "Ripple counter" where modules can be connected as shown in Figure 8 to build counter chains of any length. See Table 3 for the complete special mode list.

When the A₃/A₂ address inputs are set to 1/1, the SmartNixie module operates as a master I²C device, controlling five other slave modules to create one of two simple six digit clock designs. Figure 12 illustrates the simplest version which uses an external 50/60Hz line reference for time keeping showing time in a HH:MM:SS format. Figure 13 illustrates a slightly more complex configuration which uses a stand alone Real Time Clock IC and on board back up battery for greater than 2 years of unpowered timekeeping as well as a perpetual calendar function.

The SmartNixie modules operate from a V_{dd} from 3.0 to 5.5VDC and communicate on the I²C bus at 100Kbps. Typical supply current into V_{dd} is < 2.5mA at 5.5VDC. The nixie anode supply is 170V typical, cathode drivers are rated 240V and 100mA sink current with only 100nA of off current at 240VDC.

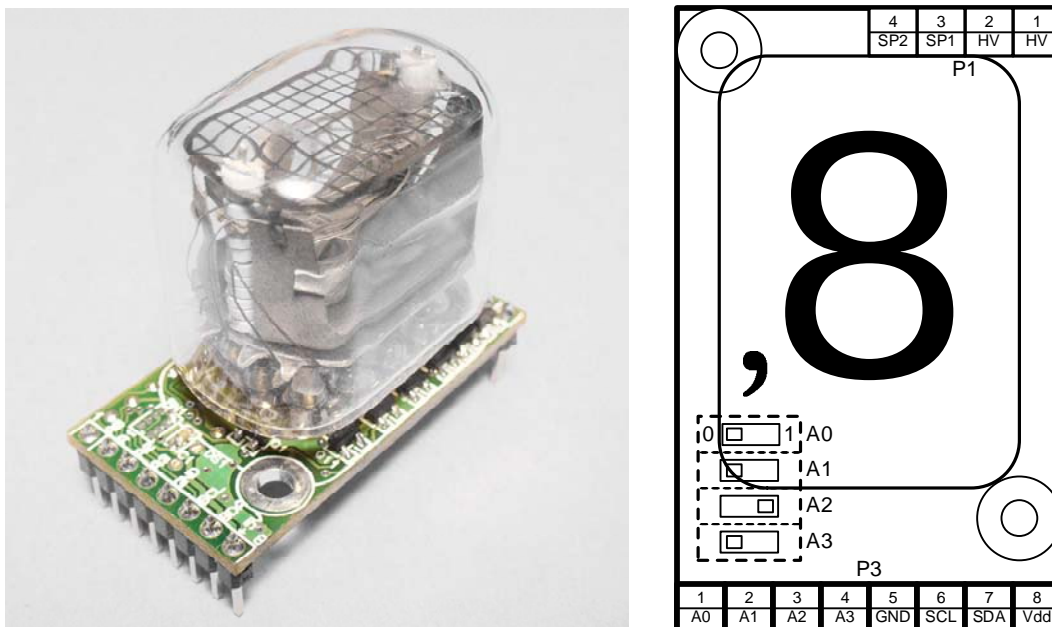


Figure 1: SmartNixie (-IN12 module shown)

Specifications: SmartNixie

Revision History

Date	FW	Affects	Description
2007/10/02	All	All	Initial release.
2008/04/27	01.02	Table 4	Changed setting entry delay from 5 to 2 seconds.
2009/02/11	N/A	Fig 8	Change reset resistor from 10K to 1K to overcome multiple module pull ups, should be >300uA per module in paralell.
	01.04	Table 3	Added Nixie/Numitron modes.
	01.04	Table 4	Added Nixie/numitron selection and new 12/24 hour display selections.
	01.04	Table 4	Added trim forward and back to adjust for slow and fast clocks.

Table 1a: Pin Descriptions -IN12

Pin	Name	Description	
P1	1	HV	+170V nixie anode voltage
	2	HV	Connected to pin 2
	3	Spare1	Comma cathode for IN12B
	4	Spare2	Aux cathode driver
P3	1	A0	Address 0 of module ¹
	2	A1	Address 1 of module ¹
	3	A2	Address 2 of module ²
	4	A3	Address 3 of module ³
	5	GND	Power input, 0V
	6	SCL	I ² C serial clock (I ² C Mode)
	7	SDA	I ² C serial data (I ² C Mode)
	8	Vdd	Power input, 3.0V-5.50V

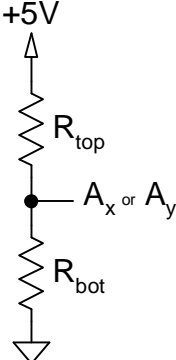
Notes:

1. When A3/A2 are 0/0, 0/1 or 1/1 these pins are configured as digital inputs pulled up to Vdd with a 50-450uA current. When A3/A2 are 1/0 these pins are configured as analog inputs with no pull ups.
2. A2 is always pulled up to Vdd with 100K.
3. A3 is always pulled up to Vdd with a 50-450uA current.

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Section 2: SmartNixie Addressing

Table 2: Module Addressing

DIP Switch				Base Addr	Description																																																																								
A ₃	A ₂	A ₁	A ₀																																																																										
0	0	0	0	0x10	Simple slave addressing, DIP switch is read as digital input with pull ups active.																																																																								
0	0	0	1	0x12																																																																									
0	0	1	0	0x14																																																																									
0	0	1	1	0x16																																																																									
0	1	0	0	0x18																																																																									
0	1	0	1	0x1A																																																																									
0	1	1	0	0x1C																																																																									
0	1	1	1	0x1E																																																																									
1	0	0	A _y			See Table 3 for special modes																																																																							
1	0	A _x	A _y	0x10-0xEE	Extended slave addressing...																																																																								
 <p>Ex Values</p> <table border="1"> <thead> <tr> <th>Bin</th> <th>Voltage</th> <th>R_{top}</th> <th>R_{bot}</th> <th>R_{tot}</th> <th>I-μA</th> </tr> </thead> <tbody> <tr><td>0</td><td>0.227</td><td>130K</td><td>6.19K</td><td>136K</td><td>37</td></tr> <tr><td>1</td><td>0.682</td><td>38.3K</td><td>6.19K</td><td>44.5K</td><td>112</td></tr> <tr><td>2</td><td>1.136</td><td>130K</td><td>38.3K</td><td>168K</td><td>30</td></tr> <tr><td>3</td><td>1.591</td><td>13.3K</td><td>6.19K</td><td>19.5K</td><td>256</td></tr> <tr><td>4</td><td>2.045</td><td>15.0K</td><td>10.0K</td><td>25.0K</td><td>200</td></tr> <tr><td>5</td><td>2.500</td><td>38.3K</td><td>38.3K</td><td>76.6K</td><td>65</td></tr> <tr><td>6</td><td>2.955</td><td>10.0K</td><td>15.0K</td><td>25.0K</td><td>200</td></tr> <tr><td>7</td><td>3.409</td><td>6.19K</td><td>13.3K</td><td>19.5K</td><td>256</td></tr> <tr><td>8</td><td>3.864</td><td>38.3K</td><td>130K</td><td>168K</td><td>30</td></tr> <tr><td>9</td><td>4.318</td><td>6.19K</td><td>38.3K</td><td>44.5K</td><td>112</td></tr> <tr><td>10</td><td>4.773</td><td>6.19K</td><td>130K</td><td>136K</td><td>37</td></tr> </tbody> </table>				Bin	Voltage	R _{top}	R _{bot}	R _{tot}	I- μ A	0	0.227	130K	6.19K	136K	37	1	0.682	38.3K	6.19K	44.5K	112	2	1.136	130K	38.3K	168K	30	3	1.591	13.3K	6.19K	19.5K	256	4	2.045	15.0K	10.0K	25.0K	200	5	2.500	38.3K	38.3K	76.6K	65	6	2.955	10.0K	15.0K	25.0K	200	7	3.409	6.19K	13.3K	19.5K	256	8	3.864	38.3K	130K	168K	30	9	4.318	6.19K	38.3K	44.5K	112	10	4.773	6.19K	130K	136K	37	<p>A_x and A_y are configured as analog inputs without pull-ups in this mode, where the unit base address can be computed from...</p> $(((\text{Bin}_{A_x} \times 11) + \text{Bin}_{A_y}) \times 2) - 2$ <p>...yielding 112 unique slave base addresses ranging from 0x10 to 0xEE.</p> <p>The Voltage Bins are defined as follows with example resistor divider values shown such that only 6 different 1% values are required:</p>	
Bin	Voltage	R _{top}	R _{bot}	R _{tot}	I- μ A																																																																								
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1	1	m	m		Clock modes, see Table 3																																																																								

Notes:

1. Voltage bins shown are based on 5V into V_{dd} but are actually ratiometric such that the same divider resistors will yield the same address/mode for any V_{dd} within the allowed operating range.

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Table 3: Module Addressing, Special Modes

DIP Switch				A _y Value			Special Mode Description: I ² C is disabled
A ₃	A ₂	A ₁	A ₀	Bin	Volts	Mode	
1	0	0	A _y	0	0.227	0	Burn-in Nixie counter free running at 10Hz (Figure 3)
				1	0.682	1	Burn-in Numitron counter free running at 10Hz (Figure 3)
				2	1.136	2	Reserved for future use
				3	1.591	3	Reserved for future use
				4	2.045	4	Reserved for future use
				5	2.500	5	Ripple counting Nixie (Figure 8)
				6	2.955	6	Ripple counting Numitron (Figure 8)
				7	3.409	7	Reserved for future use
				8	3.864	8	Version/Serial# stream on SCL, Async 19.2Kbps (Figure 11)
				9	4.318	0x10	<i>Standard mode slave address = 0x10</i>
				10	4.773	0x12	<i>Standard mode slave address = 0x12</i>
1	1	0	x	---	---	9	6 digit clock master with 60Hz reference into A ₀ (Figure 12) ³
1	1	1	x	---	---	10	6 digit clock/calendar master using PCF8563 RTC (Figure 13)

Notes:

1. Voltage bins shown are based on 5V into V_{dd} but are actually ratiometric such that the same divider resistors will yield the same address/mode for any V_{dd} within the allowed operating range.
2. Reserved mode addresses operate as the Burn-in counter mode when selected.
3. The default line frequency is 60Hz but 50, 60 and 100Hz line clock dividers are selectable via the clock setting controls.

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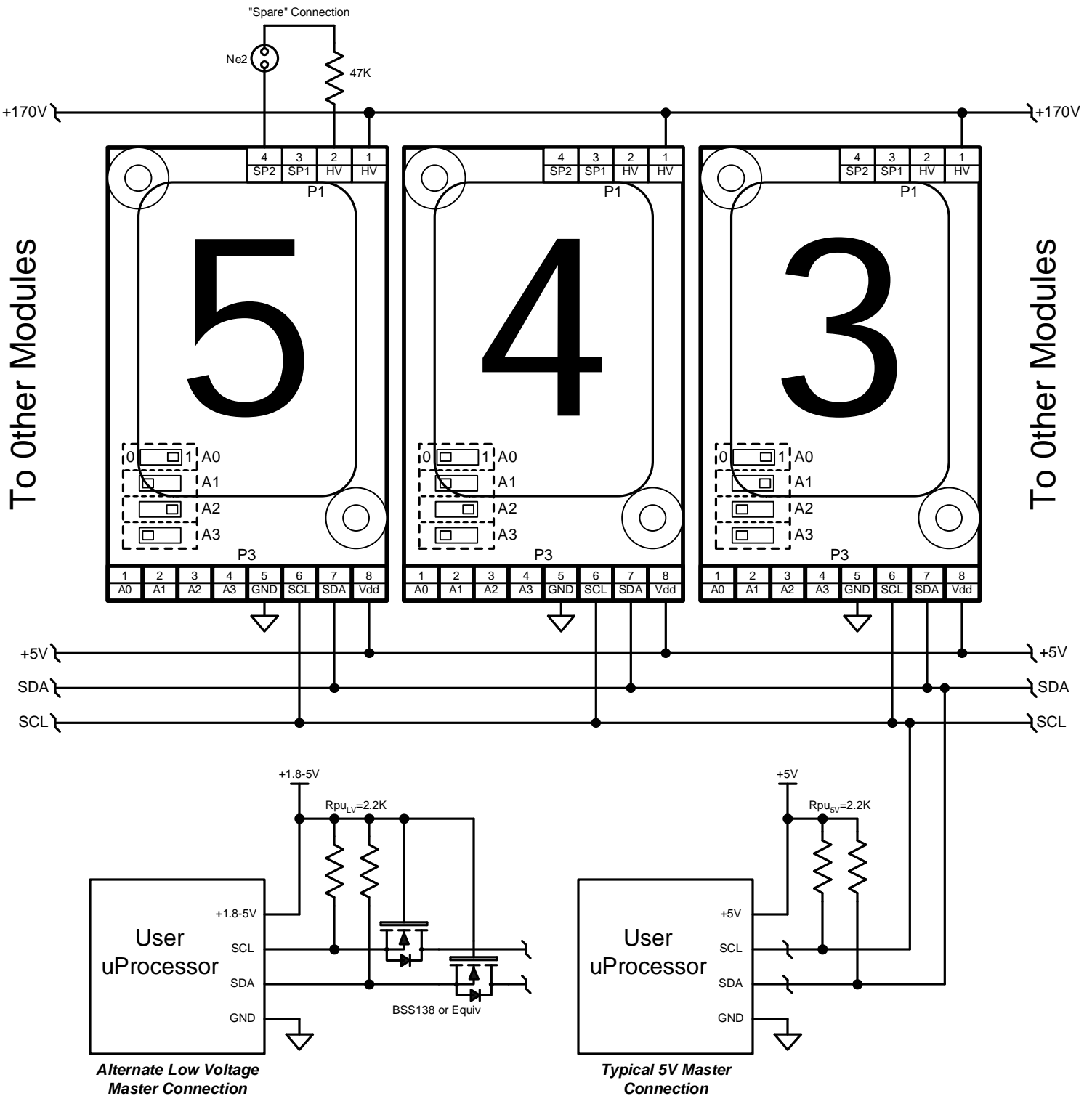
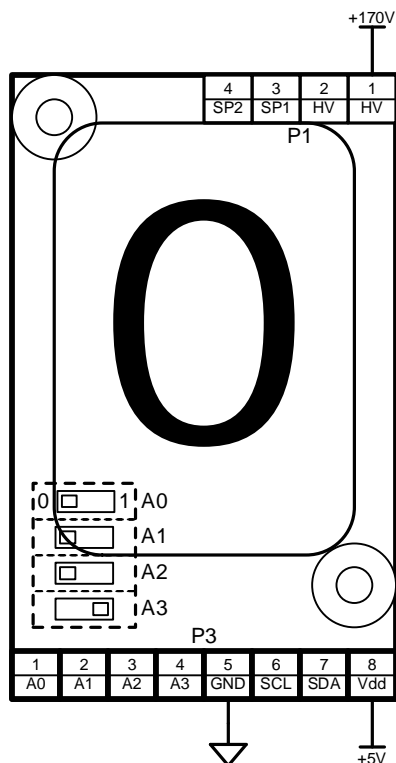


Figure 2: Typical Slave Bus Connection (Addr=0x10 to 0xEE)

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Unit will count 0-9 at
about a 10Hz rate

Figure 3: Stand Alone Burn-in Counter (Mode=0)

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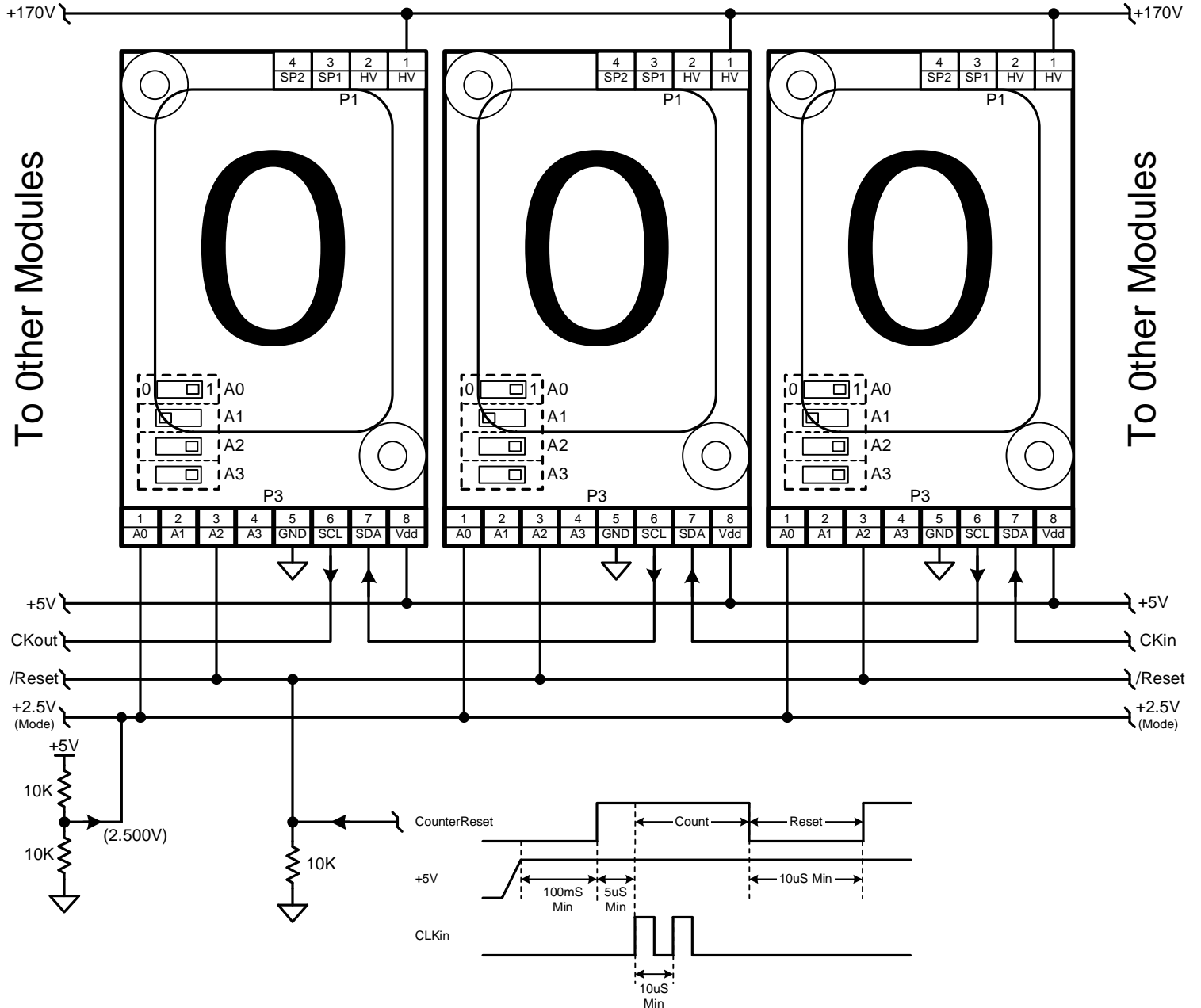


Figure 8: Ripple Counter Mode Connection, No Dimming (Mode=5)

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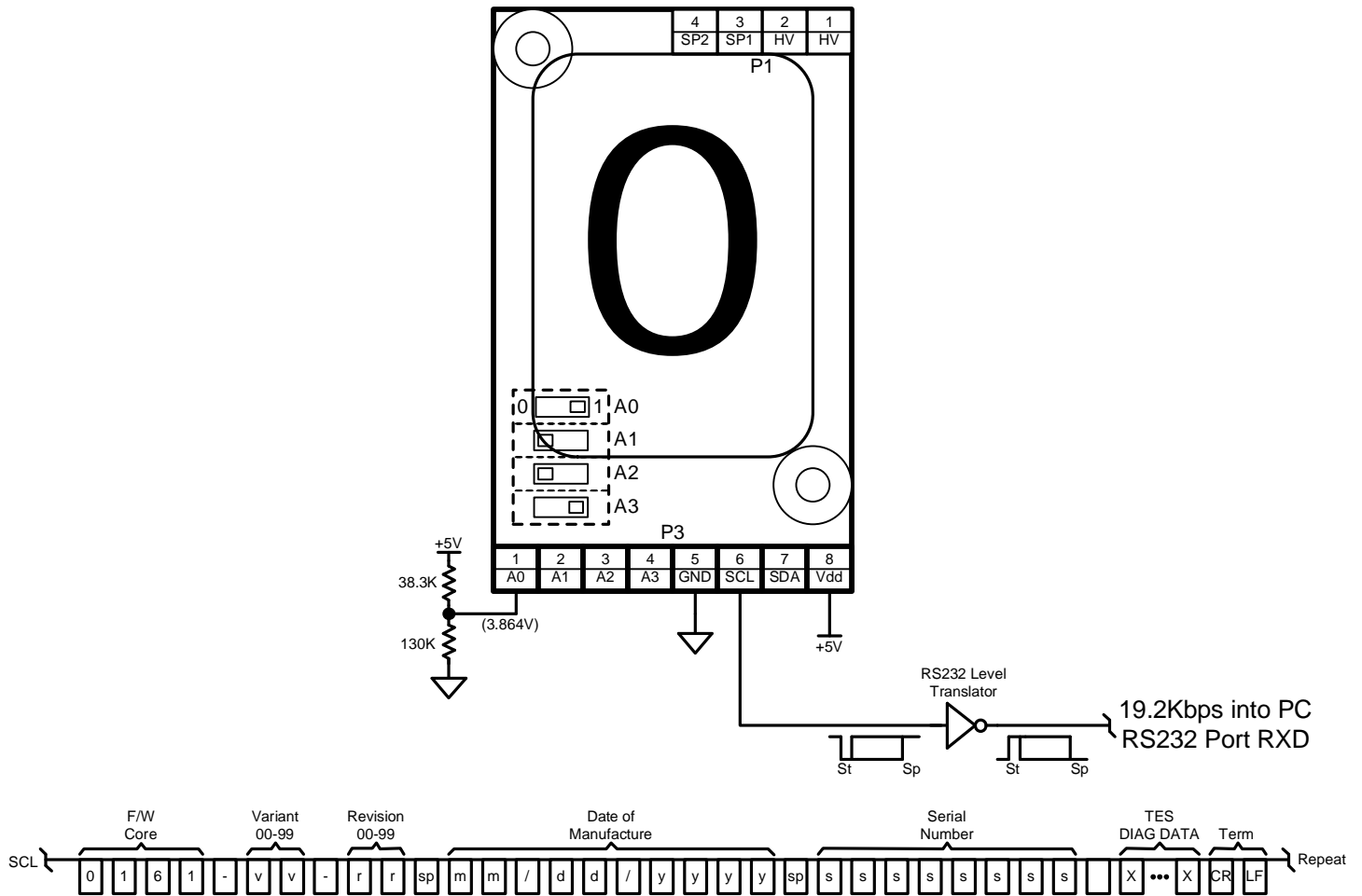


Figure 11: Serial Number / Version Data Stream (Mode=8)

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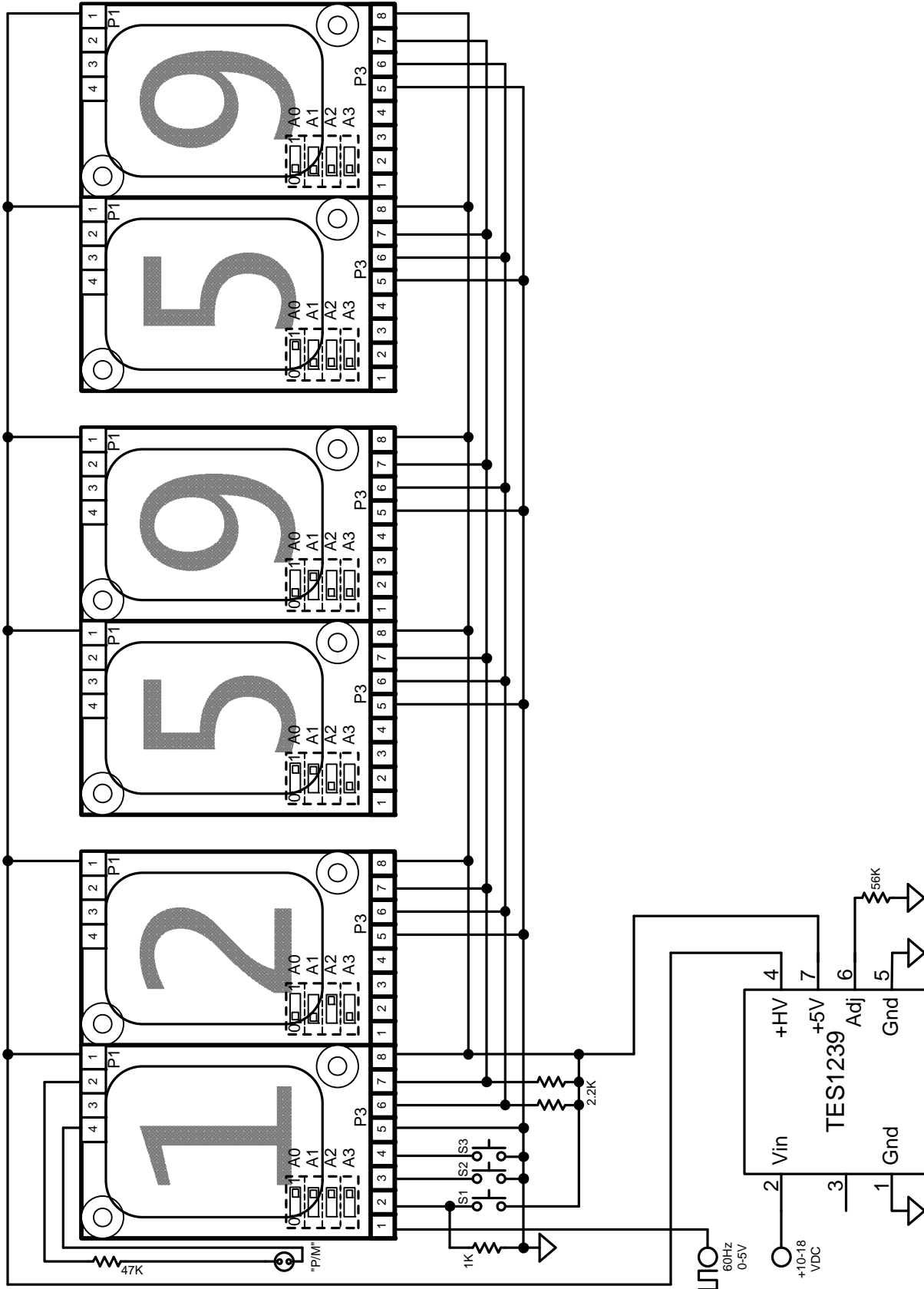


Figure 12: 60Hz Reference Clock (Mode=9)

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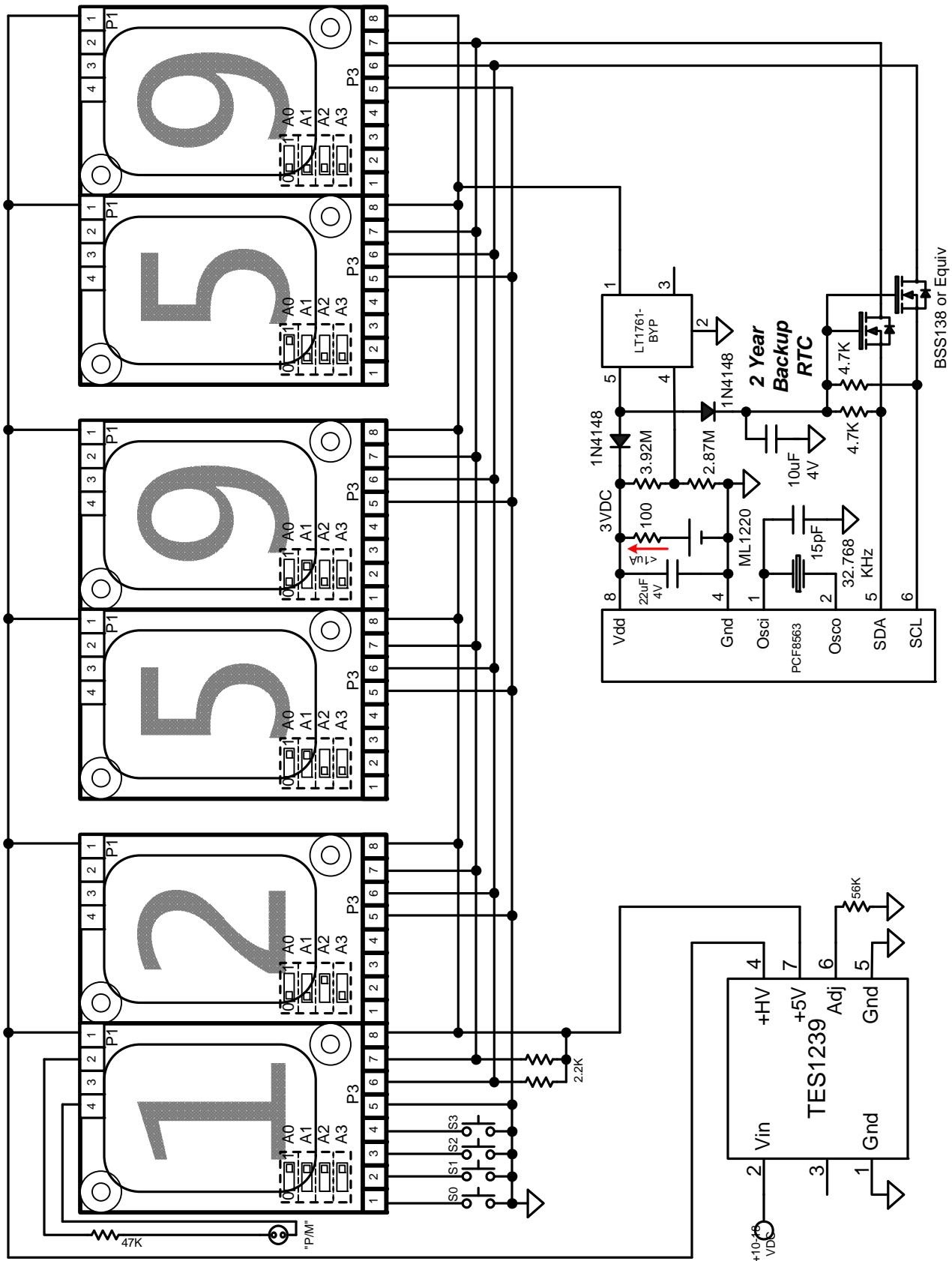


Figure 13: Stand Alone Clock/Calendar (Mode=10)

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Table 4: Clock setting (Modes 9 and 10), FW 0161.01.04

Button Press				Function Description						
S3	S2	S1	S0							
			X	Show the date in the format MM:DD:YY (Only available in RTC clock Mode 10)						
	X	X		Hold for >2 seconds to switch between Nixie and Numitron display modes						
X	X			Hold for >2 seconds to increment the current time by 1 second: Adjusts for slow clock						
X		X		Hold for >2 seconds to decrement the current time by 1 second: Adjusts for fast clock						
X				Hold for >2 seconds to enter setting mode						
X				While in setting mode, press >150mS and <2 seconds to advance to next setting selection						
				Display						
				Mode	Mode	---	---	10's	1's	Function
				0	0	---	---	H	H	Hours ¹
				0	1	---	---	M	M	Minutes
				0	2	---	---	S	S	Seconds
				0	3	---	---	Mo	Mo	Mode 10: Months
				0	4	---	---	D	D	Mode 10: Days
				0	5	---	---	Y	Y	Mode 10: Years
				0	6	---	---	C	C	12/24 hour clock display select (S1 and S2 steps through selections)
						0	1			12 hour mode, leading hours 10's zero displayed
						1	2			12 hour mode, leading hours 10's zero blanked
						0	2			24 hour mode, leading hours 10's zero displayed
						2	4			24 hour mode, leading hours 10's zero blanked
				0	7	---	---	L	L	Mode 9: Line frequency select (S1 and S2 steps through selections)
						0	0			No prescale, free-run clock
						0	1			Divide-by-1
						1	0			Divide-by-10
						5	0			Divide-by-50
						6	0			Divide-by-60
						5	2			Divide-by-100 (50 x 2)
						6	2			Divide-by-120 (60 x 2)
						9	9			Divide-by-255
				0	8	---	---	8	8	Dimmer setting, 10-100% ²
X				Hold for >2 seconds to exit setting mode, executes upon release ^{3/4}						
	X			While in the setting mode, advances the 10's digit, 150mS auto increment						
		X		While in the setting mode, advances the 1's digit, 150mS auto increment						

Notes:

- For the RTC clock (Mode 10), exiting setting when the display shows "00 xx HH" will only save the configuration data but the time will not be updated. For the line clock (Mode 9), time is updated regardless of the current setting menu since time is counted locally using the same registers to set the memory.
- "88" is displayed at the current dimming selection while the mode display remains at 100% brightness. In this mode, S2 increases and S1 decreases the brightness level in 5% steps. Upon exiting the setting mode the entire display is set to the newly selected brightness level.
- To align the clock time with an external reference: Adjust ahead to an upcoming time and then hold S3 down for more than 2 seconds. When the set time matches the reference time, release S3 to resume normal time counting.
- The Nixie/Numitron mode is saved in EEPROM and the 12/24 hour display mode, the line frequency selection and the dimmer settings are stored in EEPROM upon exiting the setting mode so that they can be reloaded when the power is cycled.
- For the GPS RTC module, after the GPS fix is acquired and time starts counting normally, adjust the clock to the current local time to allow the module to store and the automatically compute your local time zone offset.

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Section 4: SmartNixie Communication

An I²C master communicates with groups of TES1328 modules configured as slaves via a sixteen element register stack using standard I²C commands at a maximum data rate of 100kbps. See Table 5 for a complete list of the slave stack register functions.

For register writes a Start command is issued followed by the slave address where the R/W bit is cleared to zero. The next byte written is the pointer to the desired element in the register stack from 0x00 to 0x0D where this pointer is automatically trimmed to the four LSBs. The next bytes written are the register data and after the last register data byte has been sent, a Stop command is issued which completes the transaction. Each write by the master is followed by a low ACK bit generated by the slave indicating an acknowledgement of the transaction, where a high NAK bit generally indicates no slave at the specified address is present.

After each write the internal register pointer is incremented allowing from one to fourteen consecutive registers to be written in the same transaction. Writes beyond the last writable register position (0x0D) are ignored. Two byte registers are executed after the second (Low) byte has been received.

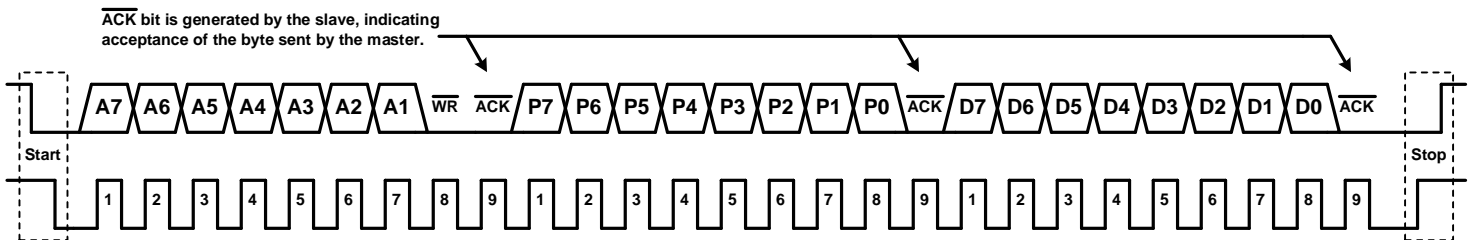


Figure 15: Typical Write Sequence

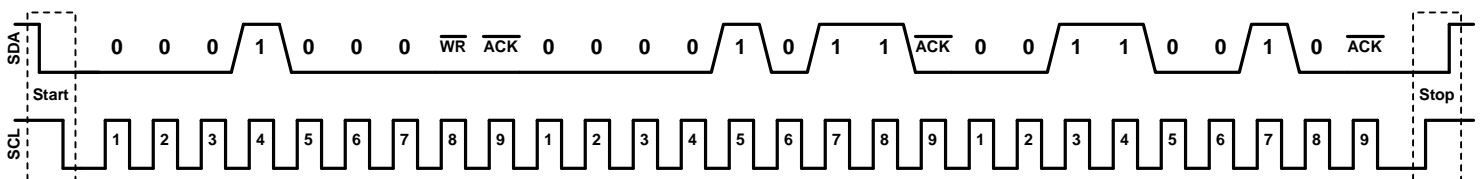


Figure 16a: Write to slave 0x10, Register 0x0B with Data 0x32 (50% dimmer)

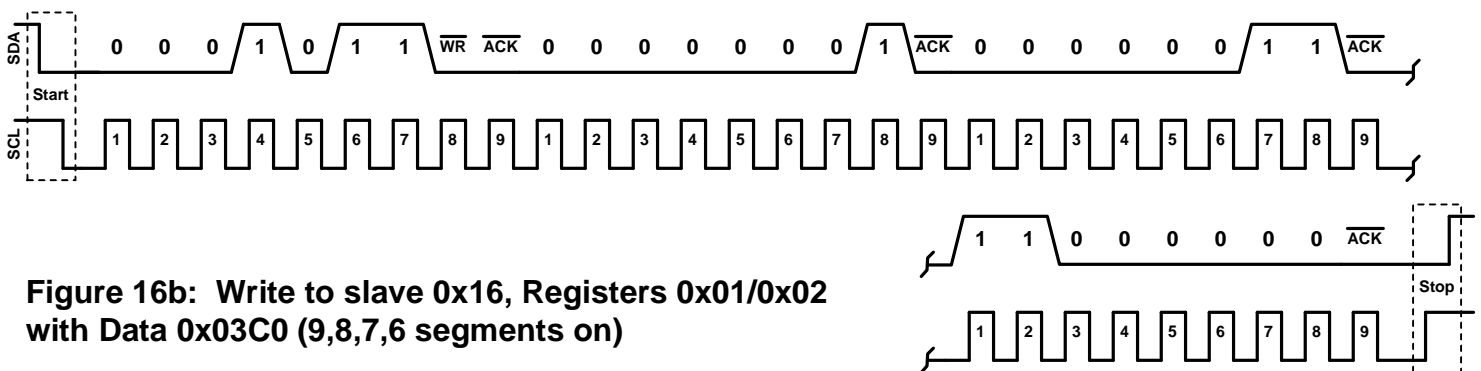


Figure 16b: Write to slave 0x16, Registers 0x01/0x02 with Data 0x03C0 (9,8,7,6 segments on)

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Section 4: SmartNixie Communication

For register reads a Start command is issued followed by the slave address where the R/W bit is set to one. The first byte read is always register 0x00 and each additional read returns the next byte in the register stack from 0x01 to 0x0F where the internal pointer is automatically trimmed to the four LSBs so that the sixteenth byte read is register 0x00 and so on. After the last register has been read by the master, a Stop command is issued which completes the transaction. Each read by the master is followed by a low ACK bit generated by the master except for the last read which must be followed by a high NAK bit from the master signaling to the slave that no further bytes will be read.

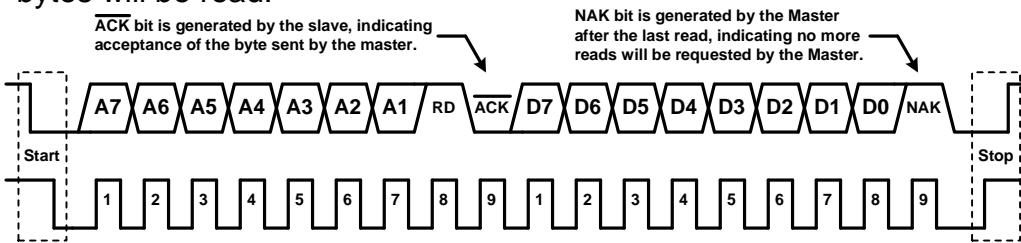


Figure 17: Typical One Byte Read Sequence

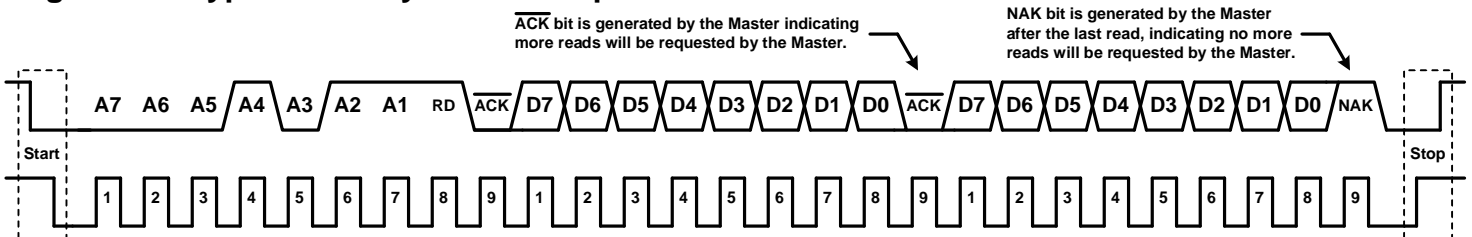


Figure 18a: Multi Byte Read Sequence from Slave 0x16

```
//PICC code for Figure 16a
I2C_START();
I2C_WRITE(0x10);           //slave address, R/W set low
I2C_WRITE(0x0B);         //register address=dimmer
I2C_WRITE(0x32);         //dimmer=50%
I2C_STOP();

//PICC code for Figure 16b
I2C_START();
I2C_WRITE(0x16);         //slave address, R/W set low
I2C_WRITE(0x01);         //register address=bitmap
I2C_WRITE(0x03);         //high byte, "9","8" on
I2C_WRITE(0xC0);         //low byte, "7","6" on
I2C_STOP();

//PICC code for Figure 18a
//Reads from slave always begin with register 0x00
I2C_START();
I2C_WRITE(0x17);         //slave address, R/W set high
data1=I2C_READ(0);       //reads register 0x00
data2=I2C_READ(1);       //reads register 0x01 (and so on)
I2C_STOP();             // last read is always (1)=NAK
```

Figure 19: Example coding

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Section 4: SmartNixie Communication

Table 5: Slave Mode Control Registers

Register	Name	Description																																																																																																																																																																																																																																																																						
0x00	Character (Nixie) <table border="1" style="margin-left: 20px;"> <tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr> <tr><td>S₂</td><td>S₁</td><td>x</td><td>B</td><td>n</td><td>n</td><td>n</td><td>n</td></tr> </table>	7	6	5	4	3	2	1	0	S ₂	S ₁	x	B	n	n	n	n	n...n 0x0-0xB displays "0"-"9", Spare1 and Spare2 0xC-0xF displays 3 segment test blocks B 1 Blanks and 0 enables the n...n display data S ₂ ,S ₁ Turns on the spare channels independently of the state of B and n...n bits																																																																																																																																																																																																																																																						
7	6	5	4	3	2	1	0																																																																																																																																																																																																																																																																	
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0x01 0x02	BitmapHigh BitmapLow	Any combination of segments can be enabled and are updated when the register BitmapLow is written. Bits marked "x" are don't care. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th colspan="8">BitmapHigh</th> <th colspan="8">BitmapLow</th> <th rowspan="2">Nixie</th> <th rowspan="2">Numitron</th> </tr> <tr> <th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th> <th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th> </tr> </thead> <tbody> <tr><td>x</td><td>x</td><td>x</td><td>x</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>"0"</td><td>Seg-A</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>x</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>"1"</td><td>Seg-B</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>x</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>"2"</td><td>Seg-C</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>x</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>"3"</td><td>Seg-D</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>x</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>"4"</td><td>Seg-E</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>x</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>"5"</td><td>Seg-F</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>x</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>"6"</td><td>Seg-G</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>x</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>"7"</td><td>Seg-DP</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>x</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>"8"</td><td>Spare-A</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>x</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>"9"</td><td>Spare-B</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>x</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Spare 1</td><td>Spare 1</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>x</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Spare 2</td><td>Spare 2</td></tr> </tbody> </table>	BitmapHigh								BitmapLow								Nixie	Numitron	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	x	x	x	x	0	0	0	0	0	0	0	0	0	0	0	0	1	"0"	Seg-A	x	x	x	x	0	0	0	0	0	0	0	0	0	0	0	1	0	"1"	Seg-B	x	x	x	x	0	0	0	0	0	0	0	0	0	0	1	0	0	"2"	Seg-C	x	x	x	x	0	0	0	0	0	0	0	0	1	0	0	0	0	"3"	Seg-D	x	x	x	x	0	0	0	0	0	0	0	1	0	0	0	0	0	"4"	Seg-E	x	x	x	x	0	0	0	0	0	0	1	0	0	0	0	0	0	"5"	Seg-F	x	x	x	x	0	0	0	0	0	1	0	0	0	0	0	0	0	"6"	Seg-G	x	x	x	x	0	0	0	0	1	0	0	0	0	0	0	0	0	"7"	Seg-DP	x	x	x	x	0	0	0	1	0	0	0	0	0	0	0	0	0	"8"	Spare-A	x	x	x	x	0	0	1	0	0	0	0	0	0	0	0	0	0	"9"	Spare-B	x	x	x	x	0	1	0	0	0	0	0	0	0	0	0	0	0	Spare 1	Spare 1	x	x	x	x	1	0	0	0	0	0	0	0	0	0	0	0	0	Spare 2	Spare 2
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x	x	x	x	0	0	0	0	0	0	0	0	0	0	0	1	0	"1"	Seg-B																																																																																																																																																																																																																																																						
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x	x	x	x	0	0	0	0	0	0	1	0	0	0	0	0	0	"5"	Seg-F																																																																																																																																																																																																																																																						
x	x	x	x	0	0	0	0	0	1	0	0	0	0	0	0	0	"6"	Seg-G																																																																																																																																																																																																																																																						
x	x	x	x	0	0	0	0	1	0	0	0	0	0	0	0	0	"7"	Seg-DP																																																																																																																																																																																																																																																						
x	x	x	x	0	0	0	1	0	0	0	0	0	0	0	0	0	"8"	Spare-A																																																																																																																																																																																																																																																						
x	x	x	x	0	0	1	0	0	0	0	0	0	0	0	0	0	"9"	Spare-B																																																																																																																																																																																																																																																						
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0x03	SevenSeg (Numitron) <table border="1" style="margin-left: 20px;"> <tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr> <tr><td>S₂</td><td>S₁</td><td>Dp</td><td>B</td><td>n</td><td>n</td><td>n</td><td>n</td></tr> </table>	7	6	5	4	3	2	1	0	S ₂	S ₁	Dp	B	n	n	n	n	n...n 0x0-0xF displays "0"-"9", "A"-"F" B 1 Blanks and 0 enables the n...n display data S ₂ ,S ₁ ,Dp Turns on the spare and decimal point channels independently of the state of B and n...n bits																																																																																																																																																																																																																																																						
7	6	5	4	3	2	1	0																																																																																																																																																																																																																																																																	
S ₂	S ₁	Dp	B	n	n	n	n																																																																																																																																																																																																																																																																	
0x04-0x05	Reserved	Reserved for future use																																																																																																																																																																																																																																																																						
0x06-0x08	EEPROM	Factory EEPROM Control Registers																																																																																																																																																																																																																																																																						
0x09-0x0A	Reserved	Reserved for future use																																																																																																																																																																																																																																																																						
0x0B	Dimmer	Display duty cycle from 0 to 100%: On time is (n x 100uS) + 100uS for a minimum illumination of 1% and a PWM frequency of 10Khz. 50% will be equal to a 10.1mS period of 50% duty cycle (~100Hz).																																																																																																																																																																																																																																																																						
0x0C	Delay	Delay in 10mS units from 10mS to 2.55S used for the free running burn-in counter mode (Count increment timer) as well as the character flash mode (On/Off timer).																																																																																																																																																																																																																																																																						
0x0D	Command	Command 0x00 Start burn-in counter 0x01 Stop burn-in counter 0x02 Start character flashing 0x03 Stop character flashing 0x96 Reset slave CPU																																																																																																																																																																																																																																																																						
0x0E	FirmwareCore	Read Only: 0161																																																																																																																																																																																																																																																																						
0x0F	FirmwareRevision	Read Only: VRR Variant (0/1/2) and Revision (00-99)																																																																																																																																																																																																																																																																						

Specifications: SmartNixie

Section 5: SmartNixie Electrical

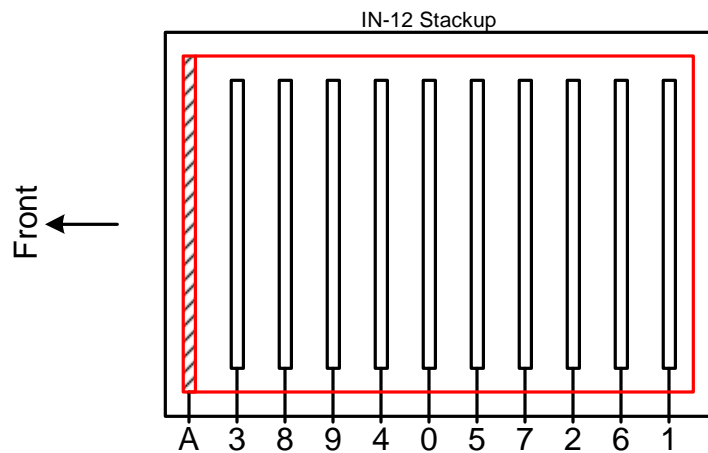
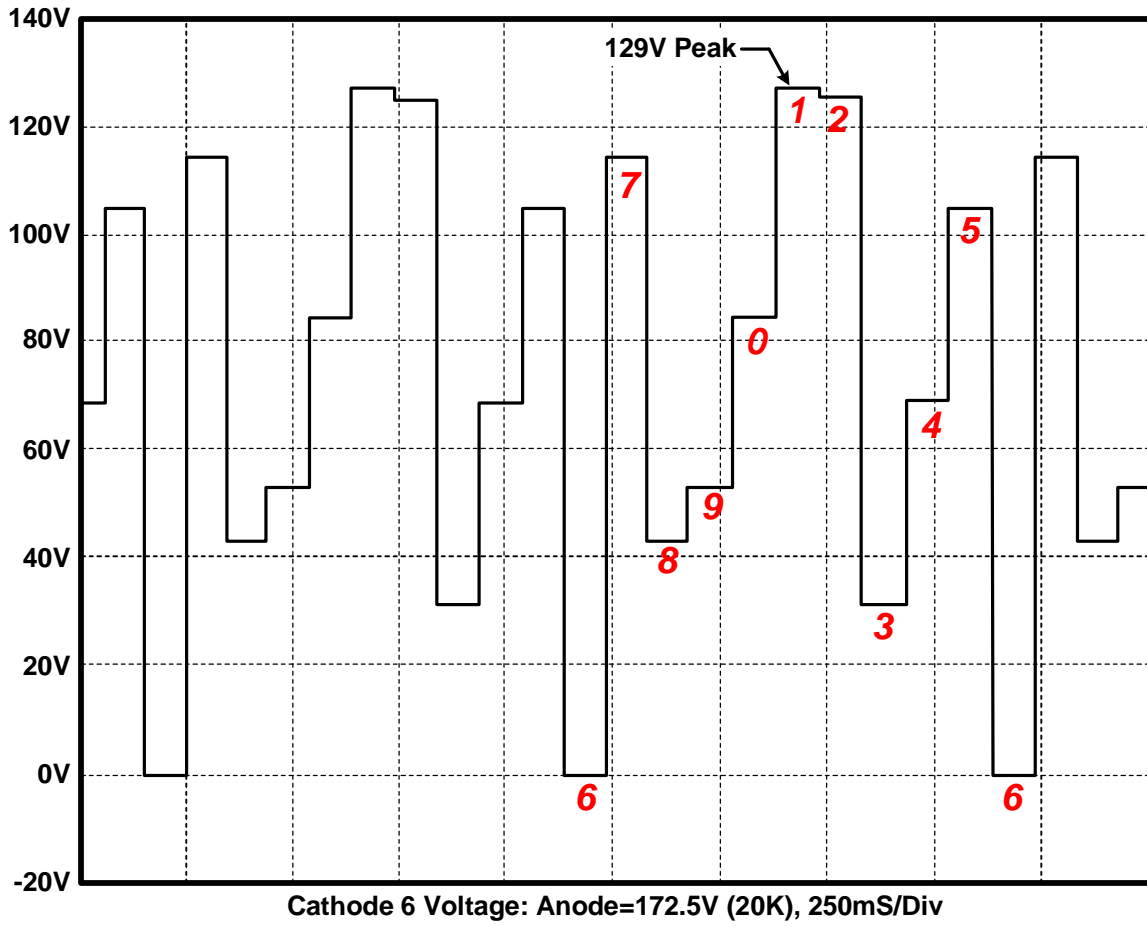


Figure 20: Burn-in Counting Mode Inter-Digit Coupling (-IN12 module signals shown)

Specifications: SmartNixie

Section 5: SmartNixie Electrical

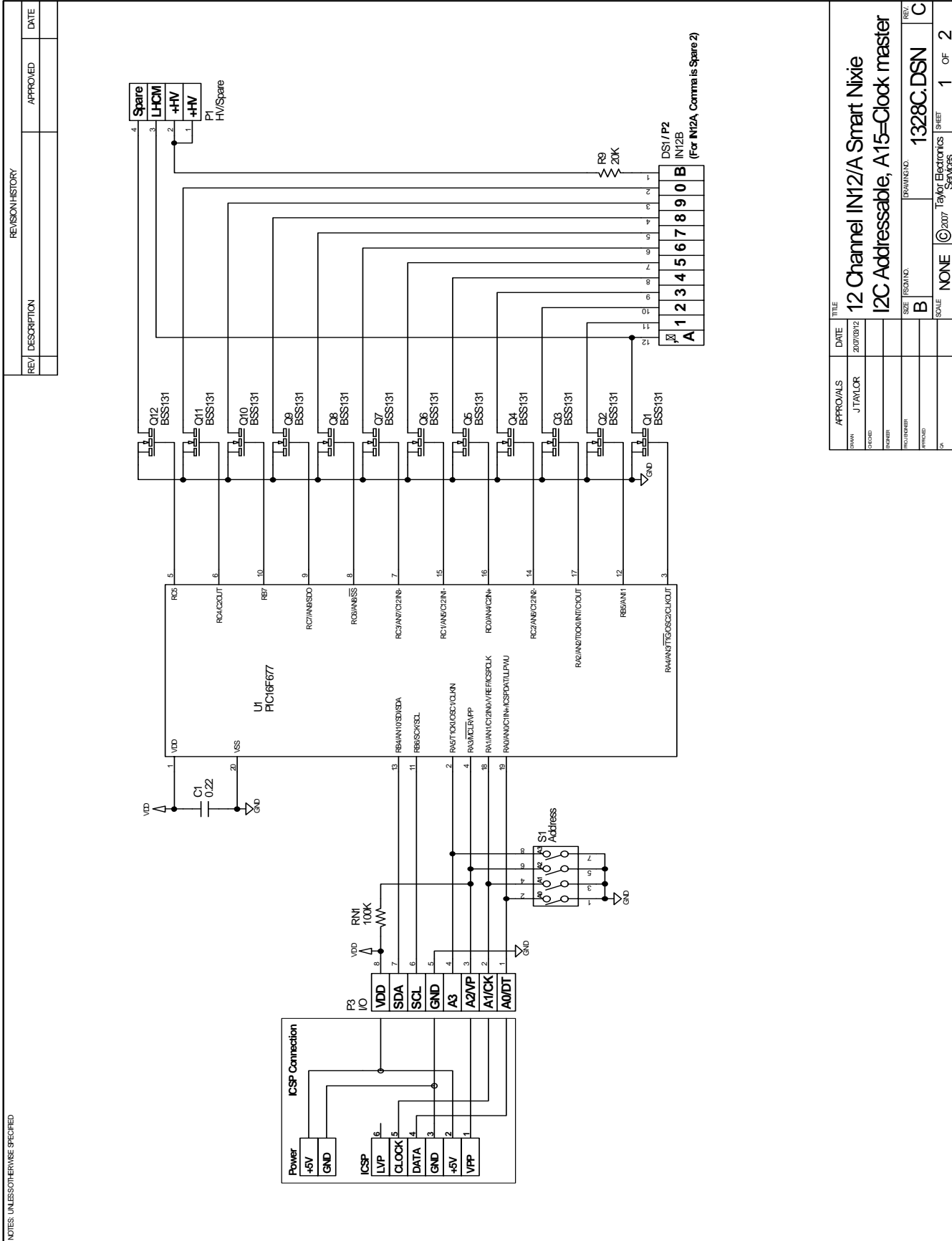


Figure 21: Schematic, SmartNixie-IN12

