

PIC12F6XX/16F6XX

5.3.2 EMBEDDING DATA MEMORY CONTENTS IN HEX FILE

The programmer should be able to read data memory information from a hex file and conversely (as an option), write data memory contents to a hex file along with program memory information and Configuration Word (0x2007) and user ID (0x2000-0x2003) information.

The 256 data memory locations are logically mapped starting at address 0x2100. The format for data memory storage is one data byte per address location, LSb aligned.

6.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

TABLE 6-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated)				
		Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$				
		Operating Voltage $4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$				
Sym.	Characteristics	Min.	Typ.	Max.	Units	Conditions/Comments
General						
VDD	VDD level for read/write operations, program and data memory	2.0	—	5.5	V	
	VDD level for bulk erase operations, program and data memory	2.0 4.5	— —	5.5 5.5	V V	PIC12F6XX/16F6XX-ICD PIC12F6XX/16F6XX
VIHH	High voltage on $\overline{\text{MCLR}}$ for Program/Verify mode entry	10	—	13	V	
TVHHR	MCLR rise time (V_{SS} to V_{HH}) for Program/Verify mode entry	—	—	1.0	μs	
TPDP	Hold time after V_{PP} changes	5	—	—	μs	
VIH1	(ICSPCLK, ICSPDAT) input high level	$0.8 V_{DD}$	—	—	V	
VIL1	(ICSPCLK, ICSPDAT) input low level	$0.2 V_{DD}$	—	—	V	
TSET0	ICSPCLK, ICSPDAT setup time before $\overline{\text{MCLR}}\uparrow$ (Program/Verify mode selection pattern setup time)	100	—	—	ns	
THLD0	Hold time after V_{DD} changes	0	—	2	μs	
Serial Program/Verify						
TSET1	Data in setup time before clock \downarrow	100	—	—	ns	
THLD1	Data in hold time after clock \downarrow	100	—	—	ns	
TDLY1	Data input not driven to next clock input (delay required between command/data or command/command)	1.0	—	—	μs	
TDLY2	Delay between clock \downarrow to clock \uparrow of next command or data	1.0	—	—	μs	
TDLY3	Clock \uparrow to data out valid (during a Read Data command)	—	—	80	ns	
TERA	Erase cycle time	—	5	6	ms	
TPROG1	Programming cycle time (internally timed)	3	—	—	ms	Program memory Data memory
		6	—	—	ms	
TPROG2	Programming cycle time (externally timed)	3	—	—	ms	$10^{\circ}\text{C} \leq T_A \leq +40^{\circ}\text{C}$ Program memory
TDIS	Time delay from program to compare (HV discharge time)	100	—	—	μs	